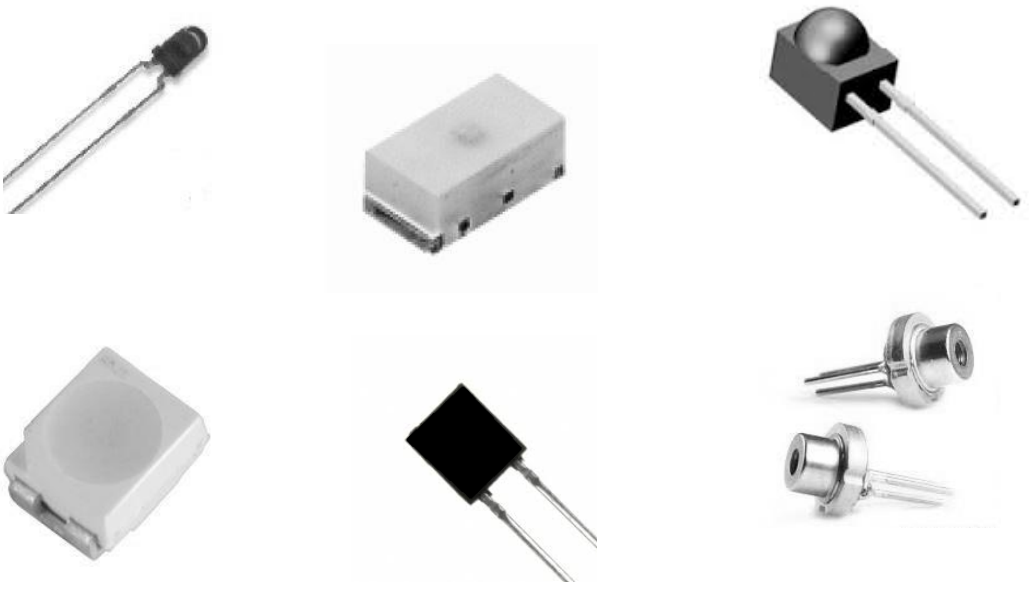
**AEC - Q102 - Rev A**
**April 6, 2020**

# FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR OPTOELECTRONIC SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS



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**Attachments**

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## Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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# FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR OPTOELECTRONIC SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS

***Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures and tables have also been revised, but changes to these areas have not been underlined.***

***Unless otherwise stated herein, the date of implementation of this standard for new qualifications and re-qualifications is as of the publish date above.***

## 1. SCOPE

This document defines the minimum stress test driven qualification requirements and references test conditions for qualification of optoelectronic semiconductors (e.g., light emitting diodes, photodiodes, laser components (see Figure 1a & b)) in all exterior and interior automotive applications. It combines state of the art qualification testing, documented in various documents (e.g., JEDEC, IEC, MIL-STD) and manufacturer qualification standards.

The qualification of multichip modules using optoelectronic functions together with other components (e.g., LEDs with integrated circuits, laser components with photodiodes, optocoupler) is described in Attachment AEC-Q102-003. (The document is not released at the time of the release of the AEC-Q102 rev. A main document, it is expected to be available in 2020)

This document does not relieve the supplier of their responsibility to meet their own company's internal qualification program. Additionally, this document does not relieve the supplier from meeting any user requirements outside the scope of this document. In this document, "user" is defined as any company developing or using an optoelectronic semiconductor part in production. The user is responsible to confirm and validate all qualification and assessment data that substantiates conformance to this document.

### 1.1 Purpose

The purpose of this document is to determine that a part is capable of passing the specified stress tests and thus can be expected to give a certain level of quality / reliability in the application.

### 1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents.

#### 1.2.1 Automotive

AEC-Q001 Guidelines for Part Average Testing
AEC-Q002 Guidelines for Statistical Yield Analysis
AEC-Q005 Pb-Free Test Requirements
SAE/USCAR-33 Specification for testing LED Modules
ZVEI Guideline for Customer Notifications of Product and/or Process Changes (PCN) of Electronic Components specified for Automotive Applications
The following document from AEC-Q101 is respectively valid also for qualification of optoelectronic semiconductors according to AEC-Q102:
AEC-Q101-005 Electrostatic Discharge Test - Charged Device Model

### 1.2.2 Industrial

JEDEC JESD-22 Reliability Test Methods for Packaged Devices
J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.
JESD51-50 Overview of Methodologies for the Thermal Measurement of Single- and Multi-Chip Single- and Multi-PN Junction Light-Emitting Diodes (LEDs)
JESD51-51 Implementation of the Electrical Test Method for the Measurement of Real Thermal Resistance and Impedance of Light-Emitting Diodes with Exposed Cooling
JESD51-52 Guidelines for Combining CIE 127-2007 Total Flux Measurements with Thermal Measurements of LEDs with Exposed Cooling Surface
ANSI/ESDA/JEDEC JS-001 Human Body Model (HBM) - Component Level
IEC 60068-2-43 Hydrogen sulphide test for contacts and connections
IEC 60068-2-20 Test methods for solderability and resistance to soldering heat of devices with leads
IEC 60068-2-58 Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)
IEC 60068-2-60 Flowing mixed gas corrosion test

### 1.2.3 Military

MIL-STD-750-1 Environmental Test Methods for Semiconductor Devices
MIL-STD-750-2 Mechanical Test Methods for Semiconductor Devices

### 1.2.4 Other

IATF 16949 Quality management system requirements for automotive production and relevant service parts organizations

## 1.3 Definitions

### 1.3.1 AEC-Q102 Qualification

Successful completion and documentation of the test results from requirements outlined in this document allows the supplier to claim that the part is “AEC-Q102 qualified”. The supplier, in agreement with the user, can perform qualification at sample sizes and conditions less stringent than what this document requires. However, that part cannot be considered “AEC-Q102 qualified” until such time that the unfulfilled requirements have been successfully completed.

For ESD, it is highly recommended that the passing voltage be specified in the supplier datasheet with a footnote on any pin exceptions. Note that there are no "certifications" for AEC-Q102 qualification and there is no certification board run by AEC to qualify parts.

The minimum temperature range for optoelectronic semiconductors per this document shall be -40ºC up to the maximum operating temperature defined in the part specification.

### 1.3.2 Approval for Use in an Application

"Approval" is defined as the user’s approval for use of a part in their application. The user’s method of approval is beyond the scope of this document.

### 1.3.3 Terminology

In this document, “part” refers to the same entity as would “device” or “component” that is a singulated light emitting diode (containing one or multiple dies), photo diode, photo transistor, etc., with a packaged die or an unpackaged die with solderable terminations for board attachment. It can be designed in various ways, sometimes using an integrated protection device for electrostatic discharge (e.g., ESD-diode). Not meant for bare die, needing an additional connection step (e.g., wire bonding of top contact) after the soldering process.

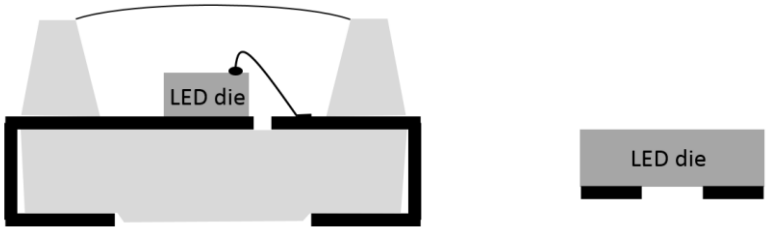



**Figure 1a: Examples of Light Emitting Diodes**

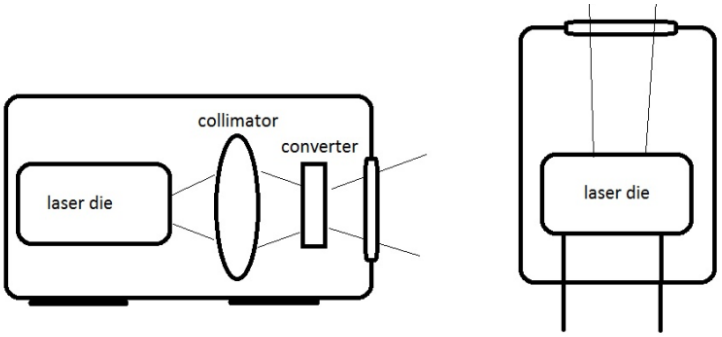



**Figure 1b: Examples of Laser Components**

**Note:** The term “laser component” within this document includes an assembled singular pure laser die as well as an assembled combination of laser die, collimator, and converter.

## 2. GENERAL REQUIREMENTS

### 2.1 Precedence of Requirements

In the event of conflict in the requirements of this document and those of any other documents, the following order of precedence applies:

a. The purchase order
b. The individual agreed upon part specification
c. This document
d. The reference documents in Section 1.2 of this document
e. The supplier's data sheet

For the part to be considered qualified per this document, the purchase order and/or individual part specification cannot waive or detract from the requirements of this document.

### 2.2 The Use of Generic Data to Satisfy Qualification and Re-qualification Requirements

The use of generic (family) data to simplify the qualification/re-qualification process is encouraged. To be considered, the generic data must be based on the following criteria:

a. Part qualification requirements listed in Table 2.
b. Matrix of specific requirements associated with each characteristic of the part and manufacturing process as shown in Table 3a-c.
c. Definition of family guidelines established in Appendix 1.
d. Represent a random sample of the normal population.
e. Use of high risk parts within a product/process family.

Appendix 1 defines the criteria by which parts are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable to the qualification of the part in question.

With proper attention to these qualification family guidelines, information applicable to other parts in the family can be accumulated. This information can be used to demonstrate generic reliability of a part family and minimize the need for part-specific qualification test programs. This can be achieved through qualification of a range of parts representing the “four corners” of the qualification family (e.g., highest/lowest current, minimum/maximum amount of dies, etc.). Sources of generic data should come from supplier-certified test labs, and can include internal supplier's qualifications, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions, sample size and number of lots specified in Table 2.

Table 1 provides guidelines showing how the available part test data may be applied to reducing the number of lots required for qualification. Parametric verification to the individual user part specification must be performed for each part submission, generic characterization data is not allowed. Whenever appropriate generic data can be used, the supplier has to give a rationale to the user(s). **The user(s) will be the final authority on the acceptance of generic data in lieu of specific part test data.**

| Part Information | Lot Requirements for Qualification |
|---|---|
| New part, no applicable generic data. | Lot and sample size requirements per Table 2. |
| A part in a family is qualified. The part to be qualified is less complex and meets the Family Qualification Definition per Appendix 1. | Only part specific tests as defined in Section 4.2 are required. Lot and sample size requirements per Table 2 for the required tests. |
| A new part that has some applicable generic data. | Review Section 2.2 above to determine required tests from Table 2. Lot and sample sizes per Table 2 for the required tests. |
| Part process change. | Review Tables 3a-c to determine which tests from Table 2 should be considered. Lot and sample sizes per Table 2 for the required tests. |
| Qualification/Requalification involving multiple sites or families | Refer to Appendix 1, Section 3. |

**Table 1: Part Qualification/Re-qualification Lot Requirements**

Table 2 defines a set of qualification tests that must be considered for both new part qualifications and re-qualification associated with a design or process change.

Tables 3a-c define a matrix of appropriate qualification tests that must be considered for any changes proposed for the part. Tables 3a-c are the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and the user should use as a baseline for discussion of tests that are required for the qualification/requalification in question. **It is the supplier's responsibility to present and document rationale for why any of the highlighted tests need not be performed.**

### 2.3 Test Samples

#### 2.3.1 Lot Requirements

Lot requirements are designated in Table 2, herein. If more than one lot is required, all lots have to be chosen randomly (when possible) from die manufacturing and assembly.

#### 2.3.2 Production Requirements

All qualification parts shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at projected production volumes.

#### 2.3.3 Reusability of Test Samples

Parts that have been used for nondestructive qualification tests may be used to populate other qualification tests. Parts that have been used for destructive qualification tests may not be used any further except for engineering analysis.

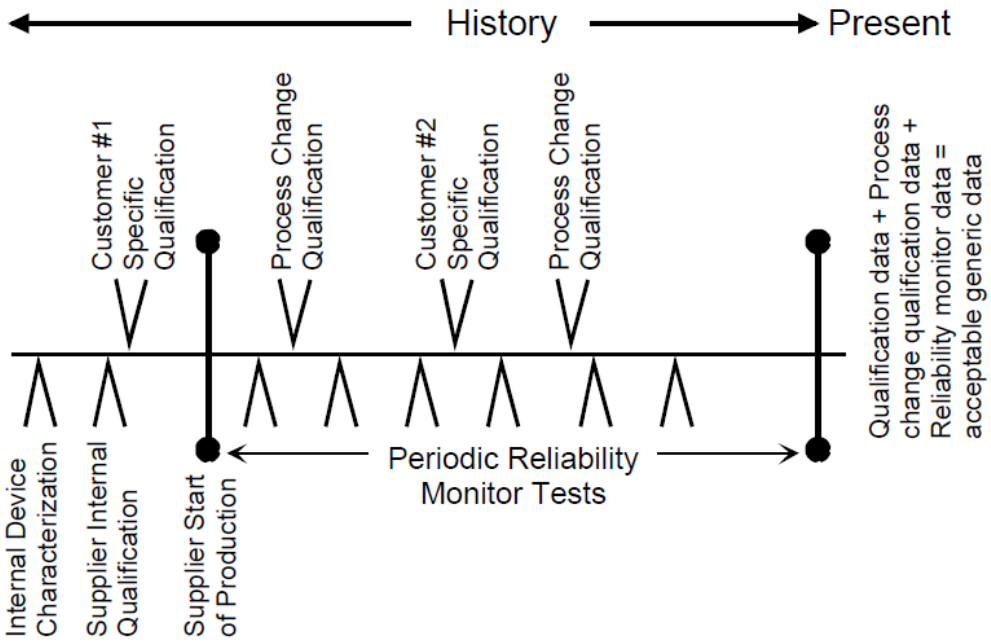
#### 2.3.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2. If the supplier elects to submit generic data for qualification/requalification, the specific test conditions and results must be reported. Existing applicable generic data should first be used to satisfy these requirements and those of Section 2.2 for each test requirement in Table 2. Part specific qualification testing should be performed if the generic data does not satisfy these requirements.

The supplier must perform any combination of the specific part to be qualified and/or an acceptable generic part(s) that totals a minimum of pieces as defined in Table 2.

#### 2.3.5 Time Limit for Acceptance of Generic Data

There are no time limits for the acceptability of generic data as long as the appropriate reliability data is submitted to the user for evaluation. Use the diagram below for appropriate sources of reliability data that can be used. This data must come from the specific part or a part in the same qualification family, as defined in Appendix 1. Potential sources of data could include any user specific data (withhold user's name), process change qualification, and periodic reliability monitor data (see Figure 2).




**Note:** Some process changes may affect the use of generic data such that data obtained before these types of changes will not be acceptable for use as generic data.

**Figure 2: Generic Data Time Line**

### 2.3.6 Assembly on Test Boards

If the parts have to be mounted on test boards, the supplier shall make an appropriate choice of process and materials, which shall be documented in the test report.

It is recommended to prove the quality of the interconnection by adequate methods (e.g., X-ray, Rth measurement, Vf measurement, etc.) prior to stress testing.

### 2.3.7 Pre- and Post-Stress Test Requirements

Electrical and optical parameters as defined in Appendix 5 have to be measured before and after the stress testing at the nominal test conditions as mentioned in the appropriate part specification. For LEDs and laser components, the forward voltage has to be measured also at the minimum (or lower) and maximum specified drive current. If no minimum drive current is specified, 10% of the nominal current or ≤1mA should be chosen. For photodiode and phototransistor components the reverse dark current has to be measured at specified reverse voltage as mentioned in the appropriate part specification.

All pre- and post-stress test parts must be tested to the electrical characteristics defined in the individual user part detail specification at room temperature.

**In addition, a simple functioning/no functioning test (e.g., LEDs: light/no light, photodiode: open/short) at minimum and maximum allowed temperature (with an allowed tolerance of +/- 5°) according to the manufacturer datasheet is mandatory for the following stress tests: WHTOL/H³TRB, TC, PTC/IOL, CA-VVF-MS, H2S and FMG**

**The functioning/no functioning test is not applicable for laser components without casting (e.g., hermetic metal can (TO)) and pulse laser components with multiple bond wire operated at high currents. For all other laser components, the functioning/no functioning test can simply be verified by an open/short check below threshold.**

**The functioning/no functioning test for photodiodes can be verified by a simple open/short check.**

**The functioning/no functioning test for phototransistors can be verified by using a simple pragmatic illumination (e.g., bulb, torch). No quantitative results needed.**

**The functioning/no functioning test must only be done after the stress tests. It is not necessary for intermediate read-outs.**

**Alternatively, a failure detection during stress testing is possible.**

### 2.4 Definition of Test Failure after Stressing

Test failures are defined as parts exhibiting any of the following criteria:

a. Parts not meeting the electrical and optical test limits defined in the part specification. Minimum test parametric requirements shall be as specified in Appendix 5.

b. Parts not remaining within ± x% (as defined in Appendix 5) of the initial reading of each test after completion of environmental testing. Parts exceeding these requirements must be justified by the supplier and approved by the user. For leakages below 100nA, tester accuracy may prevent a post stress analysis to initial reading.

c. Any part exhibiting physical damage attributable to the environmental test (migration, corrosion, mechanical damage, delamination, other). For detection use optical microscope having magnification capability of up to 50X. Note that some physical damage may mutually be agreed by the supplier and the user as only non-functional defect with no effect on the part.

If the cause of failure is agreed (by the manufacturer and the user) to be due to mishandling, interconnect to the test board, ESD or some other cause unrelated to the test conditions, the failure shall be discounted after failure analysis, but reported as part of the data submission. Nevertheless, it is necessary that as many parts passed the tests as defined for the sample size in Table 2. That's why it is recommended to start the test with more samples than needed and/or choose an appropriate test board. If testing more samples than required and at least one part failed, this must be reported.

### 2.5 Criteria for Passing Qualification/Re-qualification

Passing all appropriate qualification tests specified in Table 2, either by performing the tests (acceptance of zero failures using the specified minimum sample size) on the specific part or demonstrating acceptable family generic data (using the family definition guidelines defined in Appendix 1 and the total required lot and sample sizes), qualifies the part per this document.

Parts that have failed the acceptance criteria of tests required by this document require the supplier to satisfactorily determine root cause, implement and verify the corrective action to assure the user that the failure mechanism is understood and contained. The part shall not be considered as passing stress-test qualification until the root cause of the failure is determined and the corrective and preventive actions are confirmed to be effective. New samples or data may be requested to verify the corrective action. If generic data contains any failures, the data is not usable as generic data unless the supplier

has verified corrective action for the failure condition. In any case, communication between the supplier and the user is required to determine validity of the corrective action.

It is strongly recommended to conduct deeper analysis to detect potential component weakness on tested parts that produce behavior or responses that are outside its sampling population, even if those parts are still marginally within acceptance criteria.

Any unique reliability tests or conditions requested by the user and not specified in this document shall be agreed upon between the supplier and the user requesting the test, it will not preclude a part from passing stress-test qualification as defined by this document.

### 2.6 Alternative Testing Requirements

Any deviation from the test requirements and conditions listed in Table 2 are beyond the scope of this document. Deviations (e.g., accelerated test methods) must be demonstrated to the AEC for consideration and inclusion into future revisions of this document.

See Appendix 7: Guideline on Relationship of Robustness Validation to AEC-Q102 for more information.

### 2.7 Temperature Measuring Position

For SMD parts, $T_{solder}$ is defined as the temperature measured at the hottest solder connection between the part and the board used for assembly (see Figure 3). For some parts types like "Chip on Board LED" or leaded laser components, other assembly methods like screwing or clinching are used. In this case, $T_{solder}$ can be replaced by $T_{case}$ measured at an appropriate position of the part (see Figure 3). Measuring $T_{solder}$ directly during stress testing may be very difficult for some package designs. In this case, an appropriate position to measure $T_{board}$ instead might be chosen. The position of the $T_{board}$ measurement should be chosen in the way that the thermal resistance to the $T_{solder}$ position is as low as possible. The supplier has to define and provide the used definition. In addition, the supplier has to provide the measured or calculated Ts and Tj (see Appendix 4). Note, that actual measured temperatures may deviate from the specified temperature because of additional thermal resistance of the used test setup.

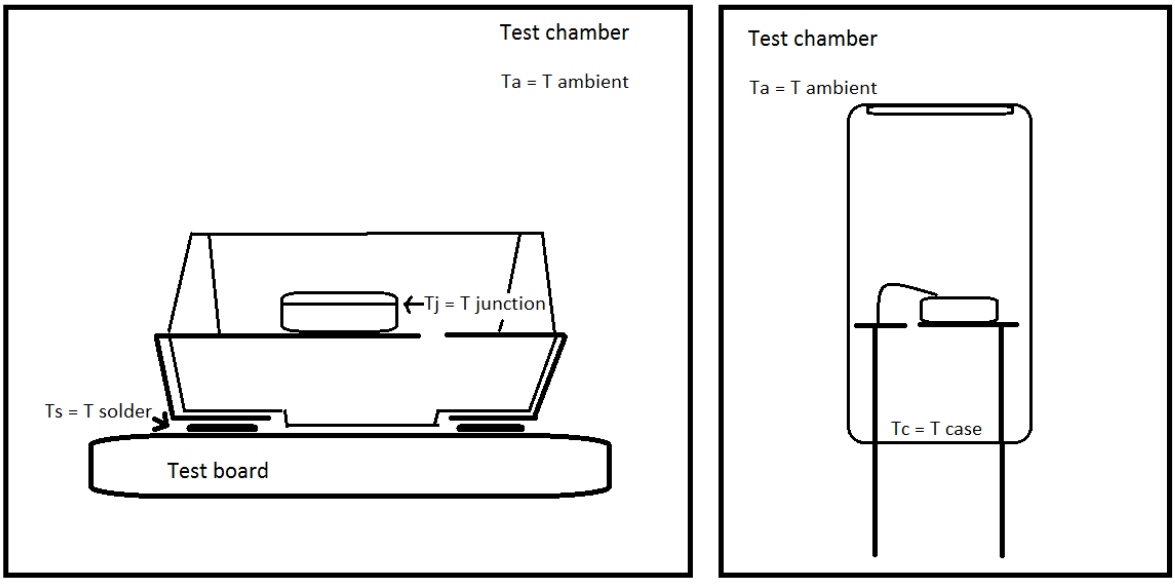



**Figure 3: Definition of $T_{ambient}$, $T_{solder}$, $T_{case}$ and $T_{junction}$. For different LED designs, the definition of the measuring points must be done respectively.**

## 3. QUALIFICATION AND REQUALIFICATION

### 3.1 Qualification of a New Part

Stress test requirements and corresponding test conditions for a new part qualification are listed in Table 2. For each qualification, the supplier must present data for all of these tests (see Appendix 4), whether it is stress test results on the specific part or acceptable generic family data. A review is to be made of other parts in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user. For each part qualification, the supplier must also present a Certificate of Design, Construction and Qualification to the requesting user. See Appendix 2.

### 3.2 Re-qualification of a Changed Part

Re-qualification of a part is required when the supplier makes a change to the product and/or process that impacts (or could potentially impact) the form, fit, function, quality and/or reliability of the part (see Tables 3a-c for guidelines).

#### 3.2.1 Process Change Notification

In addition to Tables 3a-c, the supplier will meet mutually agreed upon requirements for product/process changes.

#### 3.2.2 Changes Requiring Re-qualification

As a minimum, any change to the product, as defined above, requires performing the applicable tests listed in Table 2, using Tables 3a-c to determine the re-qualification test plan. Tables 3a-c should be used as a guide for determining which tests need to be performed.

#### 3.2.3 Criteria for Passing Requalification

All requalification failures shall be analyzed for root cause, with corrective and preventive actions established as required. The part and/or qualification family may be granted “qualification status” if, as a minimum, proper containment is demonstrated and approved by the user with corrective and preventive actions established and verified, normally via requalification and rerun the failing test until it successfully passes.

#### 3.2.4 User Approval

A change may not affect a part’s specification but may affect its performance in an application. Individual user authorization of a process change shall be based on a contract between the supplier and the user and is outside the scope of this document.

### 3.3 Qualification Test Plan

The supplier and the user may agree mutually on a signed Qualification Test Plan as soon as possible after supplier’s selection for new parts, and at the time of notification (see Section 3.2.2) prior to process changes. The Qualification Test Plan, as defined in Appendix 3, shall be used to provide a consistent method of documentation supporting what testing will be performed as required by Tables 2 & 3a-c.

## 4 QUALIFICATION TESTS

### 4.1 General Tests

Test details are given in Table 2. Not all tests apply to all parts. For example, certain tests apply only to uncasted parts. The applicable tests for the particular part type are indicated in the "Note" column and the "Additional Requirements" column of Table 2. The "Additional Requirements" column of Table 2 also serves to highlight test requirements that supersede those described in the referenced test. Any unique qualification tests or conditions requested by the user and not specified in this document shall be negotiated between the supplier and user requesting the test.

### 4.2 Part Specific Tests

The following tests must be performed on the specific part (i.e., family data is not allowed for these tests):

a. Electrostatic Discharge Characterization (Table 2, Test E3 & E4)

b. Parametric Verification (Table 2, Test E2) - The supplier must demonstrate that the part is capable of meeting parametric limits detailed in the individual user part specification.

### 4.3 Data Submission Format

A data summary shall be submitted as defined in Appendix 4. Raw data with a graphical presentation shall be submitted to the individual user upon request. **All data and documents (e.g., justification for non-performed tests, etc.) shall be maintained by the supplier in accordance with IATF 16949 requirements.**

### 4.4 Requirements for Testing Pb-free Components

The supplier shall follow the requirements of AEC-Q005 Pb-Free Test Requirements for all parts whose plating material on the leads/terminations contains <1000ppm by weight of lead (Pb).

### 4.5 Notes for Testing Laser Components

For laser components in on/off operation, condensation on the light emitting surface can lead to permanent damage of the laser component.

Special care has to be taken, that no current spikes (even very short ones) occur during operation and testing. Possible reasons could be inappropriate power supplies or damaged test boards. Current spikes can easily lead to COD (Catastrophic Optical Damage).

Laser components may be operated in ACC (Automatic Current Control) mode or also APC (Automatic Power Control) mode. The additional requirements in Table 2 and the failure criteria in Appendix 5 mention only the ACC mode. Nevertheless, if the laser component is intended for APC mode, it is allowed to substitute “current” with “power” respectively.

In addition, laser components can be operated in constant mode or pulsed mode. In this document the term “pulsed operated” is used only for laser components, designed for and operated with very short pulse length, typically ns to ps (e.g., used for LIDAR applications). Here, the electrical driver unit typically has to be very close to the laser component (i.e., inside the climatic chamber). If the electrical driver unit is in the package itself, consider AEC-Q102-003 for optoelectronic multichip modules. Note that many electrical driver units may not withstand extended operation under these conditions.

For laser components with longer pulse length, typically ms and above, the tests used for laser components with constant mode operation apply in this document.

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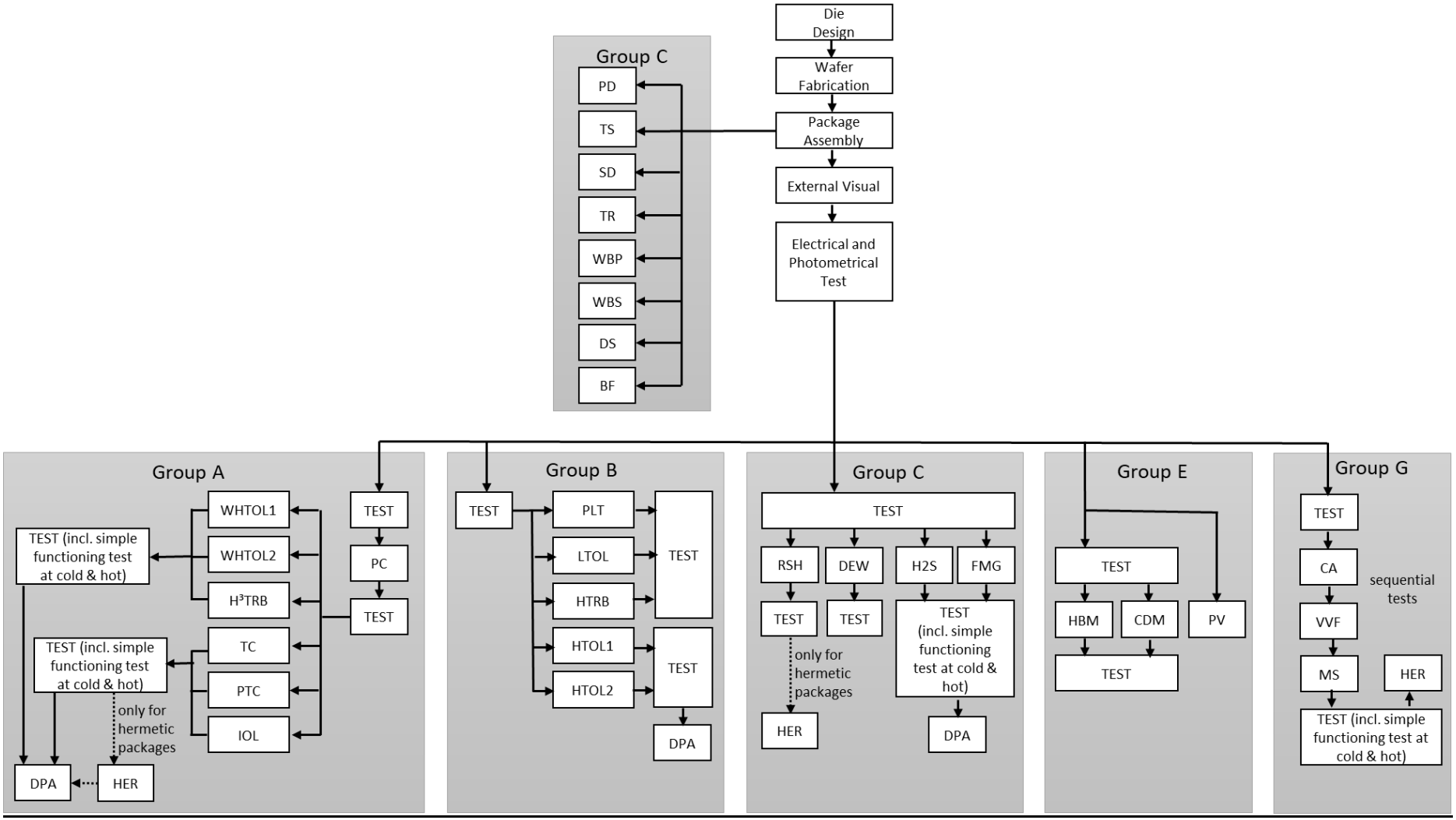


**Figure 4: Q102 Stress Test Flowchart**

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## Table 2: Qualification Test Methods

| TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| A1 | **Pre-conditioning** | **PC** | G, S | SMD qualification parts at least before Test A2a-c, A3a-b, & A4 | | 0 Fails | JEDEC JESD22-A113 | Performed on surface mount parts (SMDs) at least prior to Test A2a-c, A3a-b & A4. Where applicable, preconditioning level and Peak Reflow Temperature must be reported when preconditioning and/or MSL is performed. Any replacement of parts must be reported. Use soldering profile according to part specification with:<br>- max. allowed peak temperature<br>- max. allowed time at peak temperature within -5°C<br>- max. allowed time over liquidus temperature<br>- max. allowed ramp-up temperature gradient<br>- max. allowed ramp-down temperature gradient (absolute value)<br>**TEST before** (Alternatively production test data can be used to ensure use of non-defective parts for PC) **and after PC.** |
| A2a | **Wet High Temperature Operating Life** | **WHTOL 1** | D, G, X, Y | 26 | 3 | 0 Fails | JEDEC JESD22-A101 | **Only for LEDs and laser components.**<br>**PC before WHTOL1.**<br>Duration 1000 h at $T_{ambient}$ = 85 °C / 85% RH with maximum drive current according to derating curve defined in the part specification. Pulse operated laser components shall be operated at maximum stress condition (pulse current, pulse width & duty-cycle) according to part specification. Operated with power cycle 30 min on / 30 min off. LEDs and laser components using multiple emitters (e.g., RGB) must be operated with all emitters driven simultaneously.<br>**TEST before and after WHTOL1. DPA after WHTOL1.** |

## Table 2: Qualification Test Methods (continued)

| TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (CONTINUED) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| A2b | **Wet High Temperature Operating Life** | **WHTOL 2** | D, G, X, Y | 26 | 3 | 0 Fails | JEDEC JESD22-A101 | **Only for LEDs and CW laser components, not for pulsed operated laser components.**<br>**PC before WHTOL2.**<br>Duration 1000 h at $T_{ambient}$ = 85 °C / 85% RH with minimum drive current according to part specification. If no minimum rated drive current is specified, a drive current shall be chosen not to exceed a rise of 3 K for $T_{junction}$.<br>CW laser components shall be operated below threshold to avoid heating of the laser die. LEDs and laser components using multiple emitters (e.g., RGB) must be operated with all emitters driven simultaneously.<br>**TEST before and after WHTOL2. DPA after WHTOL2.** |
| A2c | **High Humidity High Temperature Reverse Bias** | **H³TRB** | D, G, Z | 26 | 3 | 0 Fails | JEDEC JESD22-A101 | **Only for photodiodes and phototransistors.**<br>**PC before H³TRB.**<br>Duration 1000 h at $T_{ambient}$ = 85 °C / 85% RH operated with continuous reverse bias:<br>Photodiodes: Vr = 0.8x maximum rated reverse voltage defined in part specification.<br>Phototransistors: Vce = 0.8x maximum rated collector emitter voltage defined in part specification.<br>Maximum specified power dissipation according to derating curve. No light exposure.<br>**TEST before and after H³TRB. DPA after H³TRB.** |

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## Table 2: Qualification Test Methods (continued)

| TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (CONTINUED) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| A3a | **Power Temperature Cycling** | **PTC** | D, G, X, Y | 26 | 3 | 0 Fails | JEDEC JESD22-A105 | **Only for LEDs and laser components.**<br>**PC before PTC.**<br>Duration 1000 temperature cycles with maximum drive current according to derating curve specified in part specification at maximum $T_{solder}$. For maximum temperature choose:<br>PTC condition 1: *max* $T_{solder}$ = 85 °C<br>PTC condition 2: *max* $T_{solder}$ = 105 °C<br>PTC condition 3: *max* $T_{solder}$ = 125 °C<br>PTC condition should be chosen closest to the operating temperature range within the appropriate part specification. Minimum temperature (during power off) as specified in part specification. Operated with power cycle 5 min on / 5 min off. PTC condition shall be mentioned in the test report.<br>Pulse operated laser components shall be operated at maximum stress condition (pulse current, pulse width & duty-cycle) according to part specification. LEDs and laser components using multiple emitters (e.g., RGB) must be operated with all emitters driven simultaneously. For use within special application; a longer test duration may be needed to ensure reliability over application lifetime. For details, see Appendix 7a "Reliability Validation for LEDs".<br>**TEST before and after PTC. DPA after PTC.**<br>**Additionally, for hermetic packages only: HER after PTC.** |

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## Table 2: Qualification Test Methods (continued)

| TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS (CONTINUED) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| A3b | **Intermittent Operational Life** | **IOL** | D, G, Z | 26 | 3 | 0 Fails | MIL-STD-750-1 Method 1037 | **Only for photodiodes and phototransistors.**<br>Only to be performed if enough power can be generated to achieve $\Delta T_J \geq 60$ °C.<br>Operated at $T_{ambient}$ = 25 °C with light exposure and:<br>• Photodiodes: Vr = maximum rated reverse voltage defined in part specification.<br>• Phototransistors: Vce = maximum rated collector emitter voltage defined in part specification.<br>but not to exceed absolute maximum ratings.<br>Number of cycles required: 60000/(x+y) with:<br>x = the minimum amount of minutes it takes for the part to reach the required $\Delta T_J$ from ambient temperature.<br>y = the minimum amount of minutes it takes for the part to cool to ambient temperature from required $\Delta T_J$.<br>**TEST before and after IOL. DPA after IOL.**<br>**Additionally, for hermetic packages only: HER after IOL.** |
| A4 | **Temperature Cycling** | **TC** | D, G | 26 | 3 | 0 Fails | JEDEC JESD22-A104 | **PC before TC.**<br>Duration 1000 cycles. Minimum soak & dwell time 15 min.<br>Minimum and maximum temperature as specified in part specification. The supplier ***may*** use the following recommended standardized conditions if they exceed or are equal to the storage temperature according to the appropriate part specification:<br>TC condition 1: *max* $T_{solder}$ = 85 °C<br>TC condition 2: *max* $T_{solder}$ = 100 °C<br>TC condition 3: *max* $T_{solder}$ = 110 °C<br>TC condition 4: *max* $T_{solder}$ = 125 °C<br>TC condition 5: *max* $T_{solder}$ = 150 °C<br>TC condition and transfer time shall be mentioned in the test report.<br>**TEST before and after TC. DPA after TC.**<br>**Additionally, for hermetic packages only: HER after TC.** |

## Table 2: Qualification Test Methods (continued)

| TEST GROUP B – ACCELERATED LIFETIME STRESS TESTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| B1a | **High Temperature Operating Life** | **HTOL1** | D, G, X, Y | 26 | 3 | 0 Fails | JEDEC JESD22-A108 | **Only for LEDs and laser components.** Duration 1000 h at maximum specified $T_{solder}$. For LED and CW laser components, choose corresponding maximum drive current according to derating curve defined in the part specification. Test B1a is equivalent to B1b if no derating. Pulse operated laser components shall be operated at maximum stress condition (pulse current, pulse width & duty-cycle) according to part specification. LEDs and laser components using multiple chips (e.g., RGB) must be operated with all emitters driven simultaneously. For use within special application; a longer test duration may be needed to ensure reliability over application lifetime. For details, see Appendix 7a "Reliability Validation for LEDs". **TEST before and after HTOL1. DPA after HTOL1.** |
| B1b | **High Temperature Operating Life** | **HTOL2** | D, G, X, Y | 26 | 3 | 0 Fails | JEDEC JESD22-A108 | **Only for LEDs and CW laser component, not for pulsed operated laser components.** Duration 1000 h at maximum specified drive current. Choose maximum corresponding $T_{solder}$ according to derating curve defined in the part specification. Test B1b is equivalent to B1a if no derating. LEDs and laser components using multiple emitters (e.g., RGB) must be operated with all emitters driven simultaneously. For use within special application; a longer test duration may be needed to ensure reliability over application lifetime. For details, see Appendix 7a "Reliability Validation for LEDs". **TEST before and after HTOL2. DPA after HTOL2.** |

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## Table 2: Qualification Test Methods (continued)

| TEST GROUP B – ACCELERATED LIFETIME STRESS TESTS (CONTINUED) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| B1c | **High Temperature Reverse Bias** | **HTRB** | D, G, Z | 26 | 3 | 0 Fails | JEDEC JESD22-A108 | **Only for photodiodes and phototransistors.**<br>Duration 1000 h at maximum specified $T_{solder}$ (equivalent to $T_{ambient}$ because no self-heating if no light exposure).<br>Operated with continuous reverse bias:<br>• Photodiodes: Vr = maximum rated reverse voltage defined in part specification.<br>• Phototransistors: Vce = maximum rated collector emitter voltage defined in part specification.<br>No light exposure. Light exposure only required for Avalanche Photo Diodes.<br>**TEST before and after HTRB.**<br>* Note: Older parts, qualified according to AEC-Q101 up to rev. C, have been qualified with 0.8x maximum rated reverse / collector emitter voltage. |
| B2 | **Low Temperature Operating Life** | **LTOL** | D, G, X | 26 | 3 | 0 Fails | JEDEC JESD22-A108 | **Only for laser components.**<br>Duration 500 h at $T_{ambient}$ = min.<br>For CW laser components choose corresponding maximum drive current according to derating curve defined in the part specification. Pulse operated laser components shall be operated at maximum stress condition (pulse current, pulse width & duty-cycle) according to part specification. Operated with power cycle 5 min on / 5 min off. If the minimum temperature cannot be reached at the solder point, a longer cycle time is requested.<br>**TEST before and after LTOL.** |
| B3 | **Pulsed Life** | **PLT** | D, G, X, Y | 26 | 3 | 0 Fails | JEDEC JESD22-A108 | **Only for LEDs and laser component operated in constant mode but in addition designed for pulsed operation with longer pulse length, typically ms and above. Not for pulsed operated laser components.**<br>Duration 1000 h at $T_{solder}$ = 55 °C ($T_{solder}$ = 25 °C for interior LEDs alternatively possible).<br>Operated with pulse width 100 µs and duty cycle 3%.<br>Maximum pulse height according to part's specification. LEDs and laser components using multiple emitters (e.g., RGB) must be operated with all emitters driven simultaneously.<br>**TEST before and after PLT.** |

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## Table 2: Qualification Test Methods (continued)

| TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| C1 | **Destructive Physical Analysis** | **DPA** | D, G | 2 (for each test) | 1 | 0 Fails | Appendix 6 | Random sample of parts that have successfully completed TC, PTC/IOL, HTOL, WHTOL/H³TRB, H2S, and FMG. (2 samples each). Provide also reference pictures. |
| C2 | **Physical Dimension** | **PD** | N, G | 10 | 3 | 0 Fails | JEDEC JESD22-B100 | Verify physical dimensions to the applicable user part packaging specification for dimensions and tolerances. |
| C3 | **Wire Bond Pull** | **WBP** | D, G, W, E | 10 bonds from min of 5 parts | 3 | 0 Fails | MIL-STD-750-2 Method 2037 | Data may be provided within PPAP ($C_{pk}$ > 1.67). |
| C4 | **Wire Bond Shear** | **WBS** | D, G, W, E | 10 bonds from min of 5 parts | 3 | 0 Fails | JESD22-B116 | Data may be provided within PPAP ($C_{pk}$ > 1.67). Acceptance criteria: (minimum shear force value ÷ ball bond area) ≥ 61N/mm² or 4gf/mil². |
| C5 | **Die Shear** | **DS** | D, G | 5 | 3 | 0 Fails | MIL-STD-750-2 Method 2017 | Data may be provided within PPAP ($C_{pk}$ > 1.67). |
| C6 | **Terminal Strength** | **TS** | D, G, L | 10 | 3 | 0 Fails | MIL-STD-750-2 Method 2036 | Evaluate lead integrity of through hole leaded parts only. |
| C7 | **Dew** | **DEW** | D, G, X, Y | 26 | 3 | 0 Fails | AEC-Q102-001 | **Only for LEDs and laser components, not for hermetic packages.** Operated with minimum drive current according to part specification. If no minimum rated drive current is specified, a drive current shall be chosen not to exceed a rise of 3 K for $T_{junction}$. CW laser components shall be operated below threshold to avoid heating of laser components die. For pulse laser components no power operation or operating at maximum stress is recommended. LEDs and laser components using multiple emitters (e.g., RGB) must be operated with all emitters driven simultaneously. **TEST before and after DEW.** |

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## Table 2: Qualification Test Methods (continued)

| TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS (CONTINUED) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| C8 | **Resistance to Solder Heat** | **RSH (-wave)** | D, G | 10 | 3 | 0 Fails | Lead containing devices per JESD22-B106<br>Lead (Pb)-free devices per AEC-Q005 | No separate RSH (-reflow) test needed because already covered by test A1 (Pre-conditioning).<br>Only for through hole leaded parts and if the supplier declared the part to be solderable by wave soldering.<br>**TEST before and after RSH.**<br>**Additionally, for hermetic packages only: HER after RSH.** |
| C9 | **Thermal Resistance** | **TR** | D, G | 10 | 1 | 0 Fails | JEDEC<br>JESD51-50<br>JESD51-51<br>JESD51-52 | **For LEDs and laser components. For photodiodes and phototransistor only if enough power can be generated to achieve $\Delta T_J \geq 60$ °C.**<br>Measure thermal resistance according to JESD51-50, JESD51-51, and JESD51-52 to assure specification compliance. |
| C10 | **Solderability** | **SD** | D, G | 10 | 3 | 0 Fails | JEDEC J-STD-002<br>or<br>IEC 60068-2-58 (SMD)<br>IEC 60068-2-20 (Through hole) | Preconditioning / accelerated ageing required. Use 155°C dry heat for 4 hours (JEDEC J-STD-002 condition category E or IEC 60068-2-20 ageing 3a).<br>For SMD use:<br>- JEDEC J-STD-002: test S1 - surface mount process simulation<br>or<br>- IEC 60068-2-58: method 2 – reflow<br>The supplier shall provide a detailed test report on request. |
| C11 | **Whisker Growth** | **WG** | G | see test method | see test method | see test method | AEC-Q005 | **Only for parts with Sn-based lead finishes.**<br>Test to be done on a family basis (plating metallization, lead configuration). |

## Table 2: Qualification Test Methods (continued)

| TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS (CONTINUED) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| C12 | **Hydrogen Sulphide** | **H2S** | D, G | 26 | 3 | 0 Fails | IEC 60068-2-43 | **Corrosion class A:** (preferred)<br>Duration 336 h at 40 °C and 90% RH.<br>$H_2S$ concentration: 15ppm<br>**Corrosion class B:** (acceptable for some application)<br>Duration 500 h at 25 °C and 75% RH.<br>$H_2S$ concentration: 10ppm<br>The corrosion class has to be mentioned clearly in the test report.<br>No corrosion allowed. If the supplier can show by means of additional testing or analysis that the corrosion has no impact on product reliability and lifetime, the device may be considered as passed. Nevertheless, the corrosion has to be mentioned within the test report. Details of additional testing or analysis have to be provided to the user if requested.<br>**TEST before and after H2S. DPA after H2S.** |
| C13 | **Flowing Mixed Gas** | **FMG** | D, G | 26 | 3 | 0 Fails | IEC 60068-2-60 Test method 4 | **Duration** 500 h at 25 °C and 75% RH.<br>$H_2S$ concentration: 10ppb<br>$SO_2$ concentration: 200ppb<br>$NO_2$ concentration: 200ppb<br>$Cl_2$ concentration: 10ppb<br>No corrosion allowed. If the supplier can show by means of additional testing or analysis that the corrosion has no impact on product reliability and lifetime, the device may be considered as passed. Nevertheless, the corrosion has to be mentioned within the test report. Details of additional testing or analysis have to be provided to the user if requested.<br>**TEST before and after FMG. DPA after FMG.** |
| C14 | **Board Flex** | **BF** | D, G, S | 10 | 3 | 0 Fails | AEC-Q102-002 | Not for through-hole leaded parts.<br>If the electrical testing of a pulsed operated laser component is not possible because of a broken electronic circuit integrated on test board, it is sufficient to perform an electrical go/no go test only. |

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## Table 2: Qualification Test Methods (continued)

| TEST GROUP E – ELECTRO-OPTICAL VERIFICATION TESTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| E0 | **External Visual** | **EV** | N, G | All qualification parts submitted for testing except DPA and PD | | 0 Fails | JEDEC JESD22-B101 | Inspect part construction, marking and workmanship. |
| E1 | **Pre- and Post-Stress Electrical and Photometric Test** | **TEST** | N, G | All qualification parts tested per the requirements of the appropriate part specification. | | 0 Fails | Section 2.3.7 & User specification or supplier's standard specification | Test is performed as specified in the applicable stress reference. |
| E2 | **Parametric Verification** | **PV** | N | 26 | 3 Note A | 0 Fails | Individual AEC user specification | Test all parameters according to the part specification over the part temperature range to insure the part specification compliance. |
| E3 | **Electrostatic Discharge Human Body Model** | **HBM** | D | 10 | 3 | 0 Fails | ANSI/ESDA/JEDEC JS-001 | **TEST before and after HBM.** |
| E4 | **Electrostatic Discharge Charged Device Model** | **CDM** | D, 1 | 10 | 3 | 0 Fails | AEC Q101-005 | CDM may not be applicable for some packages. For more details, see Note 1. **TEST before and after CDM.** |

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## Table 2: Qualification Test Methods (continued)

| TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| # | STRESS | ABV | NOTES | SAMPLE SIZE / LOT | NUMBER OF LOTS | ACCEPT CRITERIA | TEST METHOD (current revision) | ADDITIONAL REQUIREMENTS |
| G1 | **Constant Acceleration** | **CA** | D, G, U (seq1) | Sample size: 10 pcs from 3 lots each<br>Items G1 through G4 are sequential tests (seq1 to seq4) for uncasted packages<br>(See Note U and H) | | 0 Fails | MIL-STD-750-2 Method 2006 | 2000 g-force (gravity units) for 1 minute. Stress shall be applied to each of three mutually perpendicular axes in plus and minus directions.<br>**TEST before and after CA, alternatively TEST before CA and after MS only.**<br>If the electrical testing of a pulsed operated laser component is not possible because of a broken electronic circuit, integrated on test board, it is sufficient to perform an electrical go/no go test only. |
| G2 | **Vibration Variable Frequency** | **VVF** | D, G, U (seq2) | | | 0 Fails | JEDEC JESD22-B103 Condition 1 | **TEST before and after VVF, alternatively TEST before CA and after MS only.** |
| G3 | **Mechanical Shock** | **MS** | D, G, U (seq3) | | | 0 Fails | JEDEC JESD22-B110 | 1500 g's for 0.5 ms, 5 blows, 3 orientations.<br>**TEST before and after MS, alternatively TEST before CA and after MS only.** |
| G4 | **Hermeticity** | **HER** | D, G, H (seq4) | | | 0 Fails | JEDEC JESD22-A109 | Fine and Gross leak test per individual user specification. |

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## LEGEND FOR TABLE 2

Notes:

- A For parametric verification data, sometimes circumstances may necessitate the acceptance of only one lot by the user. Should a subsequent user decide to use a previous user's qualification approval, it will be the subsequent user's responsibility to verify an acceptable number of lots were used.
- D Destructive test, parts are not to be reused for qualification or production.
- E Ensure that each size wire is represented in the sample size.
- G Generic data allowed. See Section 2.2.
- L Required for leaded parts only.
- N Nondestructive test, parts can be used to populate other tests or they can be used for production.
- S Required for surface mount parts only.
- U Required only for uncasted parts. These are parts with (in terms of mechanical stress) critical subcomponents (e.g.: wire bonds), that are not surrounded and covered by rigid or flexible material (typically epoxy or silicone) to avoid free vibration. Items G1 through G4 are performed as a sequential test to evaluate mechanical integrity of packages containing internal cavities. Number in parentheses below notes indicates sequence.
- H Required for hermetic packaged parts only. Items G1 through G4 are performed as a sequential test to evaluate mechanical integrity of packages containing internal cavities. Number in parentheses below notes indicates sequence.
- W Required only for parts using internal wire bonds.
- X Required only for laser components.
- Y Required only for LED.
- Z Required only for photodiodes and phototransistors.
- 1 Small package consideration for CDM testing:
  CDM testing of small packages is very challenging. The vacuum used to hold the package in place during testing may not be effective when the package is under a few square millimeters. (The same may apply for round shape parts.) The capacitance between the device under test and the field plate is also very small, which results in very fast CDM current pulses. These pulses have non-negligible peak currents but have very fast rise times and very narrow pulse widths, making the pulses impossible to measure with standard 1 GHz measurement systems. Additionally, the total charge within the pulses is so small that CDM failures of semiconductors in very small packages have seldom been seen. For these reasons, the testing of very small packages is often not performed (as agreed between the supplier and the user) due to the difficulty of testing and the very low chance of failure. Any device or package that could not be completely CDM stressed due to package size shall be recorded.

## Tables 3a-c: Process Change Guidelines for the Selection of Tests

Tables 3a-c are based on the ZVEI "Guideline for Customer Notifications of Product and/or Process Changes (PCN) of Electronic Components specified for Automotive Applications" (DeQuMa), combined with Table 2 of this AEC-Q102 document.

Destructive Physical Analysis (see Appendix 6) has to be done after TC, PTC/IOL, HTOL, WHTOL / H³TRB, H2S, and FMG. Provide also reverence pictures.

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change. Reason for not performing a considered test must be given in the qualification plan or results.

### LEGEND FOR TABLES 3a-c

A Not applicable for Ag plated devices (Ag intended to fail for this test)
B Only if bond area/wirebond is changed/affected
C Only if dopant/implantation material is changed
D Only if dimensions are changing
E Only if min/max values are changing
F Sequence change only
H Non epoxy casted devices only
J Only for chip technology using wafer bonding
K Not applicable for Au plated devices
L Only if leadframe/substrate dimensions are changed
M Only if metal composition is changed including sequence
N Only for glued chips
O Only if process is changing
P Only if material properties are changed
Q Only if glue components are changing
R Only if marking technology changes
S Only if floor life is affected
T Only if board reliability is affected
U Only if underfill is affected
V Only for non-hermetic devices
W Only if risk of corrosion is increasing
Y Only for layer technology
Z Only if conversion technology changes
1 Only if data sheet parameters are affected
2 Only if outer dimensions are critical
3 Only for leaded parts
4 Only for hermetic parts
5 Only for uncasted parts

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## Table 3a: Process Change Guideline for LEDs

| Table 2 test number | A2 a&b | A3a | A4 | B1 a&b | B3 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | Wet High temperatur Operating Life | Power Temperature Cycling | Temperature Cycling | High Temperature Operating Life | Pulse Life Test | Physical Dimensions | Wire Bond Pull | Wire Bond Shear | Die Shear | Terminal Strenght | Dew Test | Resistance to Solder Heat | Thermal Resistance | Solderability | Whisker Growth | Hydrogen Sulphide | Flow Mixed Gas Corosion | Board Flex | ESD Characterization | Constant Acceleration | Vibration Variable Frequency | Mechanical Shock | Hermeticity | Parameter-Analysis: Comparison of current with changed device | Remarks |
| | WHTOL | PTC | TC | HTOL | PLT | PD | WBP | WBS | DS | TS | DEW | RSH | TR | SD | WG | H2S | FMG | BF | HBM/CDM | CA | VVF | MS | HER | PA | |
| **ANY** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Any change with impact on agreed upon contractual agreements | | | | | | | | | | | | | | | | | | | | | | | | | |
| Any change with impact on technical interface or processability/manufacturabiliy of customer | | | T | | | | | | | | | S,T | | | | | | | | | | | | | |
| **DATA SHEET** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of datasheet parameters/electrical specification (min./max./typ. values) and/or Pulse/DC specification | E | | E | E | E | | | | | | | S | E | | | | | | E | | | | | E | |
| Correction of data sheet | | | | | | | | | | | | | | | | | | | | | | | | | |
| Specification of additional parameters | | | | | | | | | | | | | | | | | | | | | | | | • | Formalism since this is not a product change, any addtional information. |
| **DESIGN** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Design changes in epitaxy. | • | • | - | • | • | | | | | | H | | | | | | | | • | | | | | • | |
| Design changes in routing/layout. | • | • | • | • | • | | B | B | D,M | | M | • | | | | M | M | • | | | | | | • | TR might be considered for complex die bond technologies |
| Die shrink | • | • | • | • | • | | B | B | • | | | • | • | | | | | | • | | | | | • | |
| LED package (except leadframe) | • | • | • | • | | • | B | B | D | 3 | D | • | L | T | | D | D | • | | 5 | 5 | 5 | 4 | • | |
| Design of leadframe | • | • | • | • | | • | B | B | D | 3 | | • | • | T | 2 | | | • | • | 5 | 5 | 5 | 4 | • | |
| **PROCESS - WAFER PRODUCTION** | | | | | | | | | | | | | | | | | | | | | | | | | |
| New / change of wafer substrate or carrier material | P | • | P | • | • | | | | • | | P | • | • | | | P | P | P | P | | | | | • | |
| Wafer diameter | • | | | • | • | | | | | | | • | • | | | | | | P | | | | | • | |
| New final wafer thickness | P | • | • | • | • | | B | B | • | | | | • | | | | | • | P | | | | | • | |
| Change of electrically active doping/implantation element | C | C | | • | • | | | | | | | | • | | | | | | • | | | | | • | |
| Change of stacking | • | • | F | • | • | | | | | | F | | | | | | | | • | | | | | • | |
| New / change of metallization (specifically chip frontside) | • | • | • | • | • | | • | • | | | M | | | | | M | M | D,M | M,B | | | | | • | |
| New / change of metallization (specifically chip backside) | • | • | • | • | • | | | | • | | D,M | • | D,M | | | D,M | D,M | D,M | D,M | | | | | • | |
| Change in process technique (e.g. significant process changes like lithography, etch, oxide deposition, die back surface preparation/backgrind, ...) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| Process Integrity: Tuning within specification | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of material supplier with no impact on agreed specifications | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of specified wafer process sequence (deletion and/or add. process step) | Qualification effort depends on type of change. PPAP has to be updated. | | | | | | | | | | | | | | | | | | | | | | | | |
| Change in die coating or passivaton | • | P | • | • | | | P | P | | | P | | | | | P | P | P | P | | | | | • | |
| New wafer production location or transfer of wafer production to a different not previously released location/site/subcontractor | • | | • | • | • | | • | • | • | | | • | J | | | | | | • | | | | | • | |

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## Table 3a: Process Change Guideline for LEDs (continued)

| Table 2 test number | A2 a&b | A3a | A4 | B1 a&b | B3 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | WHTOL | PTC | TC | HTOL | PLT | PD | WBP | WBS | DS | TS | DEW | RSH | TR | SD | WG | H2S | FMG | BF | HBM/CDM | CA | VVF | MS | HER | PA | Remarks |
| **PROCESS - ASSEMBLY** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of leadframe/carrier base material | • | | • | P | | | • | • | • | 3 | A | • | P,1 | • | P | A | A | • | | | | | | | Explanation to provide in case H2S test is not applicable |
| Change of leadframe/carrier finishing material (internal) | • | • | • | P | | | • | • | • | | A | • | P,1 | • | | A | A | | | | | | | | Considered H2S test for exterior applications. Explanation to provide in case H2S test is not applicable |
| Change of lead and heat slug plating material/plating thickness (external) | K | | • | P | | 1 | | | | | A | • | P,1 | • | K | A | A | | | | | | | | Explanation to provide in case H2S test is not applicable |
| Bump Material / Metall System (internal) | • | • | • | • | | | | | • | | W | • | • | | | W | W | • | | | | | | | |
| Die attach material | • | • | • | • | | | | | • | | N | • | • | | | Q | Q | • | | N | N | N | | | |
| Change of bond wire material | P,D | • | • | • | • | | • | • | | | | • | | | | P,D | P,D | | | D | D | D | | | |
| Change in material for sub-components (excluding LED chip & LED package related items) with impact on agreed specifications | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Overcoat / Underfill | P | • | • | • | • | - | | | U | | - | • | U | - | | P | P | • | - | P | P | P | | | |
| Change of mold compound/encapsulation/sealing material | • | • | - | • | P | D | | | | 3 | P | • | P | T | | P | P | • | - | D | D | D | | | |
| Change of conversion material | • | • | Y | • | P | | | | | | P | • | Y | | | P | P | • | | Y | Y | Y | | • | |
| Change of direct supplier for converter material | • | • | P | • | P | | | | | | P | • | P | | | P | P | P | | P | P | P | | • | |
| Change of converter process technology | • | • | Y | • | Z | | | | | | Z | • | Y | | | Z | Z | Z | | Y | Y | Y | | • | |
| Change of product marking | | | O | | | | | | | | | T | | T | | | | | | | | | | | |
| Change in process technique (e.g. die attach, molding, plating, trim & form,.. ) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| Process Integrity: Tuning within specification | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of direct material supplier with no impact on specification | | | | | | | | | | | | | | | | | | | | | | | | | See change of material. |
| Change of specified-assembly process sequence (additional or deletion of process step) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| New assembly location or transfer of assembly to a different not previously released location/site/subcontractor | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| **PACKING/SHIPPING** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Inner Packing/shipping specification change | | | | | | | | | | | | | | T | | | | | P | | | | | | |
| Outer Packing/shipping specification change | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of labelling | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dry pack requirement change | | | | | | | | | | | | | | | | | | | | | | | | | |

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## Table 3a: Process Change Guideline for LEDs (continued)

| Table 2 test number | A2 a&b | A3a | A4 | B1 a&b | B3 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | WHTOL | PTC | TC | HTOL | PLT | PD | WBP | WBS | DS | TS | DEW | RSH | TR | SD | WG | H2S | FMG | | HBM/CDM | | VVF | MS | | PA | Remarks |
| **EQUIPMENT** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Production from a new equipment/tool which uses a different basic technology | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process. | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | |
| Change in final test equipment type that uses a different technology | | | | | | | | | | | | | | T | | | | | • | | | | | • | Gage R&R / delta correlation |
| **TEST FLOW** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Move of all or part of electrical wafer test and/or final test to a different not previously released location/site/subcontractor | • | B | • | B | B | | B | B | B | | | • | | T | | | | | • | | | | | • | Gage R&R / delta correlation; addtional specification check |
| **Q-GATE** | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of the test coverage/testing process flow used by the supplier to ensure data sheet compliance (e.g. elimination/addition of electrical measurement/test flow block; relaxation/enhancement of monitoring procedure or sampling) | | | | | | | | | | | | | | | | | | | | | | | | • | |

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## Table 3b: Process Change Guideline for Laser Components

| Table 2 test number | A2 a&b | A3 | A4 | B1 a&b | B2 | B3 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | Wet High temperatur Operating Life | Power Temperature Cycling | Temperature Cycling | High Temperature Operating Life | Low Temperature Operating Life | Pulse Life Test | Physical Dimensions | Wire Bond Pull | Wire Bond Shear | Die Shear | Terminal Strenght | Dew Test | Resistance to Solder Heat | Thermal Resistance | Solderability | Whisker Growth | Hydrogen Sulphide | Flow Mixed Gas Corosion | Board Flex | ESD Characterization | Constant Acceleration | Vibration Variable Frequency | Mechanical Shock | Hermeticity | Parameter-Analysis: Comparison of current with changed | Remarks |
| | WHTOL | PTC | TC | HTOL | LTOL | PLT | PD | WBP | WBS | DS | TS | Dew | RSH | TR | SD | WG | HZS | FMGC | BF | HBM/CDM | CA | VVF | MS | HER | PA | |
| **ANY** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Any change with impact on agreed upon contractual agreements | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Any change with impact on technical interface or processability/manufacturabiliy of customer | | | T | | | | | | | | | | S,T | | | | | | | | | | | | | |
| **DATA SHEET** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of datasheet parameters/electrical specification (min./max./typ. values) and/or Pulse/DC specification | E | | E | E | E | E | | | | | | | S | E | | | | | | E | | | | | E | |
| Correction of data sheet | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Specification of additional parameters | | | | | | | | | | | | | | | | | | | | | | | | | • | Formalism since this is not a product change, any addtional information. |
| **DESIGN** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Design changes in epitaxy. | • | • | | • | | • | | | | | | H | | | | | | | | • | | | | | • | |
| Design changes in routing/layout. | • | • | • | • | | • | | B | B | D,M | | M | • | | | | M | M | • | | | | | | • | TR might be considered for complex die bond technologies |
| Die shrink | • | • | • | • | • | • | | B | B | • | | | • | • | | | | | | • | | | | | • | |
| Laser package (except leadframe, but including internal components) | • | • | • | • | • | | • | B | B | D | 3 | D | • | L | T | | D | D | • | | 5 | 5 | 5 | 4 | • | |
| Design of leadframe | • | • | • | • | | | • | B | B | D | 3 | | • | • | T | 2 | | | • | • | 5 | 5 | 5 | 4 | • | |
| **PROCESS - WAFER PRODUCTION** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| New / change of wafer substrate or carrier material | P, V | • | P | • | | • | | | | • | | P, V | • | • | | | P | P | P | P | | | | | • | |
| Wafer diameter | V | | | • | | • | | | | | | | • | • | | | | | | P | | | | | • | |
| New final wafer thickness | P, V | • | • | • | | • | | B | B | • | | | | • | | | | | • | P | | | | | • | |
| Change of electrically active doping/implantation element | C, V | C | | • | | • | | | | | | | | • | | | | | | • | | | | | • | |
| Change of stacking | V | • | F | • | | • | | | | | | F, V | | | | | | | | • | | | | | • | |
| New / change of metallization (specifically chip frontside) | V | • | • | • | | • | | • | • | | | M, V | | | | | M | M | D,M | M,B | | | | | • | |
| New / change of metallization (specifically chip backside) | V | • | • | • | | • | | | | • | | D,M,V | • | D,M | | | D,M | D,M | D,M | D,M | | | | | • | |
| Change in process technique (e.g. significant process changes like lithography, etch, oxide deposition, die back surface preparation/backgrind, ...) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Process Integrity: Tuning within specification | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of material supplier with no impact on agreed specifications | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of specified wafer process sequence (deletion and/or additional process step) | Qualification effort depends on type of change. PPAP has to be updated. | | | | | | | | | | | | | | | | | | | | | | | | | |
| New / change of facet passivation | V | • | • | • | • | • | | | | | | V | • | | | | P,V | P,V | | • | | | | | | |
| Change in die coating or passivaton | V | P | • | • | | | | P | P | | | P,V | | | | | P,V | P,V | P | P | | | | | • | |
| New wafer production location or transfer of wafer production to a different not previously released location/site/subcontractor | V | | • | • | | • | | • | • | • | | | • | J | | | | | | • | | | | | • | |

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## Table 3b: Process Change Guideline for Laser Components (continued)

| Table 2 test number | A2 a&b | A3 | A4 | B1 a&b | B2 | B3 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | WHTOL | PTC | TC | HTOL | LTOL | PLT | PD | WBP | WBS | DS | TS | Dew | RSH | TR | SD | WG | H2S | FMGC | BF | HBM/CDM | CA | VVF | MS | HER | PA | Remarks |
| **PROCESS - ASSEMBLY** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of leadframe/carrier base material | • | • | • | P | | | | • | • | • | 3 | A | • | P,1 | • | P | A | A | • | | | | | | | Explanation should be provided in case H2S test is not applicable |
| Change of leadframe/carrier finishing material (internal) | • | • | • | P | | | | • | • | • | | A | • | P,1 | • | | A | A | | | | | | | | H2S test should be considered for automotive exterior applications. explanation should be provided in case H2S test is not applicable |
| Change of lead and heat slug plating material/plating thickness (external) | K | | • | P | | | 1 | | | | | A | • | P,1 | • | K | A | A | | | | | | | | Explanation should be provided in case H2S test is not applicable |
| Bump Material / Metall System (internal) | • | • | • | • | | | | | | • | | W | • | • | | | W | W | • | | | | | | | |
| Die attach material | • | • | • | • | | | | | | • | | N | • | • | | | Q | Q | • | | N | N | N | | | |
| Change of bond wire material | P,D | • | • | • | | • | | • | • | | | | • | | | | P,D | P,D | | | D | D | D | | | |
| Change in material for sub-components (excluding Laser chip & Laser package related items) with impact on agreed specifications | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Overcoat / Underfill | P | • | • | • | | • | | | | U | | | • | U | | | P | P | • | | P | P | P | | | |
| Change of mold compound/encapsulation/sealing material | • | • | | • | | P | D | | | | 3 | P | • | P | T | | P | P | • | | D | D | D | 4 | | |
| Change of conversion material | • | • | Y | • | | P | | | | | | P | • | Y | | | P | P | • | | Y | Y | Y | | • | |
| Change of direct supplier for converter material | • | • | P | • | | P | | | | | | P | • | P | | | P | P | P | | P | P | P | | • | |
| Change of converter process technology | • | • | Y | • | | Z | | | | | | Z | • | Y | | | Z | Z | Z | | Y | Y | Y | | • | |
| Assembly of additional internal components (e.g. lenses) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of material and / or supplier of additional internal components (e.g. lenses) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Generation of hermeticity (e.g. welding, gluing of transmissive window) | | 4 | 4 | 4 | | | | | | | | | 4 | | | | 4 | 4 | | | 4 | 4 | 4 | 4 | | |
| Change of product marking | | | O | | | | | | | | | | T | | T | | | | | | | | | | | |
| Change in process technique (e.g., die attach, bonding, moulding, plating, trim and form, …) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Process Integrity: Tuning within specification | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of direct material supplier with no impact on specification | | | | | | | | | | | | | | | | | | | | | | | | | | See change of material. |
| Change of specified-assembly process sequence (additional or deletion of process step) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| New assembly location or transfer of assembly to a different not previously released location/site/subcontractor | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| **PACKING/SHIPPING** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Inner Packing/shipping specification change | | | | | | | | | | | | | | | T | | | | | P | | | | | | |
| Outer Packing/shipping specification change | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of labelling | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Dry pack requirement change | | | | | | | | | | | | | | | | | | | | | | | | | | |

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## Table 3b: Process Change Guideline for Laser Components (continued)

| Table 2 test number | A2 a&b | A3 | A4 | B1 a&b | B2 | B3 | C2 | C3 | C4 | C5 | C6 | C7 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | WHTOL | PTC | TC | HTOL | LTOL | PLT | PD | WBP | WBS | DS | TS | Dew | RSH | TR | SD | WG | H2S | FMGC | BF | HBM/CDM | CA | VVF | MS | HER | PA | Remarks |
| **EQUIPMENT** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Production from a new equipment/tool which uses a different basic technology | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process. | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change in final test equipment type that uses a different technology | | | | | | | | | | | | | | | T | | | | | • | | | | | • | Gage R&R / delta correlation |
| **TEST FLOW** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Move of all or part of electrical wafer test and/or final test to a different not previously released location/site/subcontractor | • | B | • | B | | B | | B | B | B | | | • | | T | | | | | • | | | | | • | Gage R&R / delta correlation; addtional specification check |
| **Q-GATE** | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Change of the test coverage/testing process flow used by the supplier to ensure data sheet compliance (e.g. elimination/addition of electrical measurement/test flow block; relaxation/enhancement of monitoring procedure or sampling) | | | | | | | | | | | | | | | | | | | | | | | | | • | |

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## Table 3c: Process Change Guideline for Photodiodes & Phototransistors

| Table 2 test number | A2c | A3b | A4 | B1c | C2 | C3 | C4 | C5 | C6 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | High Humidity High Temperature Reverse Bias | Intermittend Operating Life | Temperature Cycling | High Temperature Reverse Bias | Physical Dimensions | Wire Bond Pull | Wire Bond Shear | Die Shear | Terminal Strenght | Resist. to Solder Heat | Thermal resistance | Solderability | Whisker Growth | Hydrogen Sulphide | Flow Mixed Gas Corosion | Board Flex | ESD Characterization | Constant Acceleration | Vibration Variable Frequency | Mechanical Shock | Hermeticity | Parameter-Analysis: Comparison of current with changed device | Remarks |
| | HTRB | IOL | TC | HTRB | PD | WBP | WBS | DS | TS | RSH | TR | SD | WG | H2S | FMGC | BF | HBM/CDM | CA | VVF | MS | HER | PA | |
| **ANY** | | | | | | | | | | | | | | | | | | | | | | | |
| Any change with impact on agreed upon contractual agreements | | | | | | | | | | | | | | | | | | | | | | | |
| Any change with impact on technical interface or processability/manufacturabiliy of customer | | | T | | | | | | | S,T | | | | | | | | | | | | | |
| **DATA SHEET** | | | | | | | | | | | | | | | | | | | | | | | |
| Change of datasheet parameters/electrical specification (min./max./typ. values) and/or Pulse/DC specification | E | | E | E | | | | | | S | E | | | | | | E | | | | | E | |
| Correction of data sheet | | | | | | | | | | | | | | | | | | | | | | | |
| Specification of additional parameters | | | | | | | | | | | | | | | | | | | | | | • | Formalism since this is not a product change, any addtional information. |
| **DESIGN** | | | | | | | | | | | | | | | | | | | | | | | |
| Design changes in epitaxy. | • | • | | • | | | | | | | | | | | | | • | | | | | • | |
| Design changes in routing/layout. | • | • | • | • | | B | B | D,M | | • | | | | M | M | • | | | | | | • | TR might be considered for complex die bond technologies |
| Die shrink | • | • | • | • | | B | B | • | | • | • | | | | | | • | | | | | • | |
| Component package (except leadframe) | • | • | • | • | • | B | B | D | 3 | • | L | T | | D | D | • | | 5 | 5 | 5 | 4 | • | |
| Design of leadframe | • | • | • | • | • | B | B | D | 3 | • | • | T | 2 | | | • | • | 5 | 5 | 5 | 4 | • | |
| **PROCESS - WAFER PRODUCTION** | | | | | | | | | | | | | | | | | | | | | | | |
| New / change of wafer substrate or carrier material | P | • | P | • | | | | • | | • | • | | | P | P | P | P | | | | | • | |
| Wafer diameter | • | | | • | | | | | | • | • | | | | | | P | | | | | • | |
| New final wafer thickness | P | • | • | • | | B | B | • | | | • | | | | | • | P | | | | | • | |
| Change of electrically active doping/implantation element | C | C | | • | | | | | | | • | | | | | | • | | | | | • | |
| Change of stacking | • | • | F | • | | | | | | | | | | | | | • | | | | | • | |
| New / change of metallization (specifically chip frontside) | • | • | • | • | | • | • | | | | | | | M | M | D,M | M,B | | | | | • | |
| New / change of metallization (specifically chip backside) | • | • | • | • | | | | • | | • | D,M | | | D,M | D,M | D,M | D,M | | | | | • | |
| Change in process technique (e.g. significant process changes like lithography, etch, oxide deposition, die back surface preparation/backgrind, ...) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |
| Process Integrity: Tuning within specification | | | | | | | | | | | | | | | | | | | | | | | |
| Change of material supplier with no impact on agreed specifications | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |
| Change of specified wafer process sequence (deletion and/or add. process step) | Qualification effort depends on type of change. PPAP has to be updated. | | | | | | | | | | | | | | | | | | | | | | |

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## Table 3c: Process Change Guideline for Photodiodes & Phototransistors (continued)

| Table 2 test number | A2c | A3b | A4 | B1c | C2 | C3 | C4 | C5 | C6 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | HTRB | IOL | TC | HTRB | PD | WBP | WBS | DS | TS | RSH | TR | SD | WG | H2S | FMGC | BF | HBM/CDM | CA | VVF | MS | HER | PA | Remarks |
| **PROCESS - WAFER PRODUCTION - continued** | | | | | | | | | | | | | | | | | | | | | | | |
| Change in die coating or passivaton | • | P | • | • | | P | P | | | | | | | P | P | P | P | | | | | • | |
| New wafer production location or transfer of wafer production to a different not previously released location/site/subcontractor | • | | • | • | | • | • | • | | • | J | | | | | | • | | | | | • | |
| **PROCESS - ASSEMBLY** | | | | | | | | | | | | | | | | | | | | | | | |
| Change of leadframe/carrier base material | • | | • | P | | • | • | • | 3 | • | P,1 | • | P | A | A | • | | | | | | | Explanation to provide in case H2S test is not applicable |
| Change of leadframe/carrier finishing material (internal) | • | • | • | P | | • | • | • | | • | P,1 | • | | A | A | | | | | | | | Consider H2S test for exterior applications. Explanation to provide in case H2S test is not applicable |
| Change of lead and heat slug plating material/plating thickness (external) | K | | • | P | 1 | | | | | • | P,1 | • | K | A | A | | | | | | | | Explanation to provide in case H2S test is not applicable |
| Bump Material / Metall System (internal) | • | • | • | • | | | | • | | • | • | | | W | W | • | | | | | | | |
| Die attach material | • | • | • | • | | | | • | | • | • | | | Q | Q | • | | N | N | N | | | |
| Change of bond wire material | P,D | • | • | • | | • | • | | | • | | | | P,D | P,D | | | D | D | D | | | |
| Change in material for sub-components (excluding photodiode/transistor chip & package related items) with impact on agreed specifications | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |
| Die Overcoat / Underfill | P | • | • | • | | | | U | | • | U | | | P | P | • | | P | P | P | | | |
| Change of mold compound/encapsulation/sealing material | • | • | • | • | D | | | | 3 | • | P | T | | P | P | • | | D | D | D | | | |
| Change of product marking | | | O | | | | | | | T | | T | | | | | | | | | | | |
| Change in process technique (e.g. die attach, molding, plating, trim & form,.. ) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |
| Process Integrity: Tuning within specification | | | | | | | | | | | | | | | | | | | | | | | |
| Change of direct material supplier with no impact on specification | | | | | | | | | | | | | | | | | | | | | | | See change of material. |
| Change of specified-assembly process sequence (additional or deletion of process step) | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |
| New assembly location or transfer of assembly to a different not previously released location/site/subcontractor | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |

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## Table 3c: Process Change Guideline for Photodiodes & Phototransistors (continued)

| Table 2 test number | A2c | A3b | A4 | B1c | C2 | C3 | C4 | C5 | C6 | C8 | C9 | C10 | C11 | C12 | C13 | C14 | E3 E4 | G1 | G2 | G3 | G4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name of test / Type of change | H³TRB | IOL | TC | HTRB | PD | WBP | WBS | DS | TS | RSH | TR | SD | WG | H2S | FMGC | BF | HBM/CDM | CA | VVF | MS | HER | PA | Remarks |
| **PACKING/SHIPPING** | | | | | | | | | | | | | | | | | | | | | | | |
| Inner Packing/shipping specification change | | | | | | | | | | | | T | | | | | P | | | | | | |
| Outer Packing/shipping specification change | | | | | | | | | | | | | | | | | | | | | | | |
| Change of labelling | | | | | | | | | | | | | | | | | | | | | | | |
| Dry pack requirement change | | | | | | | | | | | | | | | | | | | | | | | |
| **EQUIPMENT** | | | | | | | | | | | | | | | | | | | | | | | |
| Production from a new equipment/tool which uses a different basic technology | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |
| Production from a new equipment/tool which uses the same basic technology (replacement equipment or extension of existing equipment pool) without change of process. | Qualification effort depends on type of change. | | | | | | | | | | | | | | | | | | | | | | |
| Change in final test equipment type that uses a different technology | | | | | | | | | | | | T | | | | | • | | | | | • | Gage R&R / delta correlation |
| **TEST FLOW** | | | | | | | | | | | | | | | | | | | | | | | |
| Move of all or part of electrical wafer test and/or final test to a different not previously released location/site/subcontractor | • | B | • | B | | B | B | B | | • | | T | | | | | • | | | | | • | Gage R&R / delta correlation; addtional specification check |
| **Q-GATE** | | | | | | | | | | | | | | | | | | | | | | | |
| Change of the test coverage/testing process flow used by the supplier to ensure data sheet compliance (e.g. elimination/addition of electrical measurement/test flow block; relaxation/enhancement of monitoring procedure or sampling) | | | | | | | | | | | | | | | | | | | | | | • | |

# Appendix 1: Definition of a Qualification Family

The qualification of a particular process will be defined within, but not limited to, the categories listed below. The supplier will provide a complete description of each process and material of significance. Valid evidence for the link between the data and the subject of qualification has to be provided by the supplier.

For parts to be categorized in a qualification family, they all must share the same major process and materials elements as defined below. For each qualification test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by rationale clearly detailing similarity). All parts using the same process and materials are to be categorized in the same qualification family for that process and are acceptable by association when one family member successfully completes qualification with the exception of the device specific requirements of Section 4.2.

Prior qualification data 3 years old or newer obtained from a part in a specific family may be extended to the qualification of subsequent parts in that family provided the supplier can insure no process changes have been made.

For broad changes that involve multiple attributes (e.g., site, material(s), process(es)), refer to Section 2.2 that allows for the selection of worst-case test vehicles to cover all the possible permutations.

## A1.1 Fab Process

Each process technology (e.g., LED, Photodiodes, etc.) must be considered and subjected to stress-test qualification separately. No matter how similar, processes from one fundamental fab technology cannot be used for the other.

Family requalification with the appropriate tests is required when the process or a material is changed. The important attributes defining a qualification family are listed below:

### A1.1.1 Wafer Fab Technology

- LEDs
- Phototransistors
- Photodiodes
- Laser components

**A1.1.2 Wafer Fab Process** - consisting of the same attributes listed below:

- Process flow
- Layout design rules
- Number of masks
- Basic epitaxial process (e.g., InGaN vs. InGaAlP)
- Lithographic process (e.g., contact vs. projection, E-beam vs. X-ray, photoresist polarity)
- Etching process (e.g., dry vs. wet etching)
- Doping process (e.g., diffusion vs. ion implantation)
- Passivation/Coating material and thickness range
- Oxidation and deposition process and thickness range
- Front/back metallization material and thickness range
- Wafer bonding and lift off process

**A1.1.3 Wafer Fab Site**

**A1.2 Assembly Process**

The processes for each package type must be considered and subjected to stress-test qualification separately. For parts to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests is required when the process or a material is changed. The supplier must submit technical justification to the user(s) to support the acceptance of generic data with package and die type, different than the part being considered for stress-test qualification. The important attributes defining a qualification family are listed below:

**A1.2.1 Package Type**

Examples include Radial, PLCC-x, Chip on Board, Chip Scale Package, etc.

**A1.2.2 Assembly Process** - consisting of the same attributes listed below:

- Leadframe base material
- Leadframe plating (internal and external to the package)
- Die attach material/method
- Wire bond material, wire diameter, and process
- Plastic mold compound or other encapsulation material
- Converter material/method

**A1.2.3 Assembly Site**

**A1.2.4 Example**

3 lots of a package family using any die structure that has the same die backside metallization will suffice for the following Qualification tests. At least one lot must come from the maximum and minimum die size (allowed by the package design rules) each.

- HTOL
- TC
- PTC
- WHTOL

### A1.3 Qualification of Multiple Families and Sites

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab family or assembly family, the qualification test vehicles should be: 1) One lot of a single part type from each of the families that are projected to be most sensitive to the changed attribute, or 2) Three lots total (from any combination of acceptable generic data and stress test data) from the most sensitive families if only one or two families exist.

Below is the recommended process for qualifying changes across many process and product families:

a. Identify all products affected by the proposed process changes.

b. Identify the critical structures and interfaces potentially affected by the proposed change.

c. Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces. Conduct a risk assessment into potential failure mechanisms. Note that steps (a) to (c) are equivalent to the creation of an FMEA.

d. Define the product groupings or families based upon similar characteristics as they relate to the technology process and package families and part sensitivities to be evaluated, and provide technical justification to document the rationale for these groupings.

e. Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products, which will address each of the potential failure mechanisms and associated failure modes.

f. Robust process capability must be demonstrated at each site (e.g., control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process step(s).

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## Appendix 2: AEC-Q102 Certification of Design, Construction and Qualification

**Supplier Name:** **Date:**

The following information is required to identify a part that has met the requirements of AEC-Q102. Submission of the required data in the format shown below is optional. **All entries must be completed; if a particular item does not apply, enter "Not Applicable".** This template can be downloaded from the AEC website at http://www.aecouncil.com.

| Item Name | Supplier Response |
|---|---|
| 1. User's Part Number: | |
| 2. Supplier Part Number/Generic Part Number: | |
| 3. Device Description: | |
| 4. Wafer/Die Fab Location & Process ID:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 5. Wafer Probe Location:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 6. Assembly Location & Process ID:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 7. Final Quality Control (Test) Location:<br>a. Facility name/plant #:<br>b. Street address:<br>c. Country: | |
| 8. ESD-protective device<br>a. Manufacturer:<br>b. Facility name/plant #: | |
| 9. Wafer/Die:<br>a. Wafer size:<br>b. Die family:<br>c. Die mask set revision & name: | |
| 10. Wafer/Die Technology Description:<br>a. Wafer/Die process technology:<br>b. Substrate material<br>c. Number of mask steps: | |
| 11. Die Dimensions:<br>a. Die width:<br>b. Die length:<br>c. Die thickness (finished): | |
| 12. Die (frontside) Metallization:<br>a. Die metallization material(s):<br>b. Number of layers:<br>c. Thickness (per layer):<br>d. % of alloys (if present): | |
| 13. Die Passivation:<br>a. Number of passivation layers:<br>b. Die passivation material(s):<br>c. Thickness(es) & tolerances: | |

| | |
|---|---|
| 14. Die Overcoat Material | |
| 15. Die Prep Backside:<br>a. Die prep method:<br>b. Die metallization:<br>c. Thickness(es) & tolerances: | |
| 16. Die Separation Method:<br>a. Kerf width (μm):<br>b. Kerf depth (if not 100% saw):<br>c. Saw method: | <br><br><br>Single ☐ Dual ☐ |
| 17. Die Attach:<br>a. Die attach material ID:<br>b. Die attach method:<br>c. Die placement diagram: | <br><br><br>See attached ☐ Not available ☐ |
| 18. Package:<br>a. Type of package (e.g., plastic, ceramic, unpackaged):<br>b. JEDEC designation (e.g. PLCC etc.): | |
| 19. Mold Compound<br>a. Mold compound supplier & ID:<br>b. Mold compound type:<br>c. Flammability rating:<br>d. Fire Retardant type/composition:<br>e. Tg (glass transition temperature)(°C):<br>f. CTE (above & below Tg)(ppm/°C): | <br><br><br>UL 94 V1 ☐ UL 94 V0 ☐<br><br><br>CTE1 (below Tg) = _____<br>CTE2 (above Tg) = _____ |
| 20. Encapsulation/Casting material:<br>a. Encapsulation material supplier & ID:<br>b. Encapsulation material type:<br>c. Tg (glass transition temperature)(°C):<br>d. CTE (above & below Tg)(ppm/°C): | |
| 21. Wire Bond:<br>a. Wire bond material:<br>b. Wire bond diameter (mils):<br>c. Type of wire bond at die:<br>d. Type of wire bond at leadframe:<br>e. Number of bonds over active area: | |
| 22. Leadframe:<br>a. Leadframe material:<br>b. Leadframe bonding plating composition:<br>c. Leadframe bonding plating thickness (μinch):<br>d. External lead plating composition:<br>e. External lead plating thickness (μinch):<br>f. External lead plating technology: | |
| 23. Board Material:<br>a. Board material supplier & ID:<br>b. Board material type:<br>c. CTE: | |
| 24. Converter:<br>a. Converter material supplier & ID:<br>b. Converter material type: | |
| 25. Thermal Resistance:<br>a. $\theta_{Junction - Ambient}$ °C/W (approx):<br>b. $\theta_{Junction - SolderJoint}$ °C/W (approx): | |

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| | |
|---|---|
| 26. Maximum Process Exposure Conditions:<br><br>a. MSL @ rated SnPb temperature:<br>b. MSL @ rated Pb-free temperature:<br><br>J-STD-020x fulfilled: | * Note: Temperatures are as measured on the center of the plastic package body top surface.<br>at °C (SnPb)<br>at °C (Pb-free)<br><br>☐ yes - revision: ☐ no |

| Attachments: | | Requirements: |
|---|---|---|
| Die Photo | ☐ | 1. A separate Certification of Design, Construction & Qualification must be submitted for each part number, wafer fab, and assembly location. |
| Package Outline Drawing | ☐ | |
| Die Cross-Section Photo/Drawing | ☐ | |
| Wire Bonding Diagram | ☐ | 2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below. |
| Die Placement Diagram | ☐ | |

| | |
|---|---|
| Completed by: Date: | Certified by: Date: |
| Typed or Printed:<br><br>Signature:<br><br>Title: | |

This template is available as a stand-alone document that can be downloaded at http://www.aecouncil.com.

## Appendix 3: AEC-Q102 Qualification Test Plan

The supplier is requested to complete and submit the Optoelectronic Semiconductor Qualification Test Plan as part of the pre-launch Control Plan whenever qualification submission is required. Acceptance and subsequent sign-off of the plan will establish a qualification agreement between the user and the supplier determining requirements for both new parts and process changes prior to commencement of testing. Where "family" data is being proposed, the plan will document how the reliability testing previously completed fulfills the requirements outlined in this document. An approved copy of the Qualification Test Plan shall be included with each qualification submission.

The test plan section of the form should detail ONLY the testing that will be performed on the specific part shown. For process change qualifications, multiple parts can be included on the same plan. Supporting generic or family data reports should be noted in the comment section and attached. When requesting use of generic or family data, attach a separate page detailing similarities or differences between parts referencing the criteria in Appendix 1. There must be valid and obvious links between the data and the subject of qualification.

The example below is provided to demonstrate how the Qualification Test Plan Form, found on the AEC website, should be used. In this case, a part was chosen as being representative of a typical new part qualification requesting reduced component testing by including generic test data. The part comes from a supplier who previously qualified the package, assembly site, etc. This example is shown for illustration purposes only and should not limit any requirements from Table 1 herein.

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## Qualification Plan acc. to AEC-Q102 for Optoelectronic Semiconductor

Rev. A

| | | | |
|---|---|---|---|
| Supplier: | *Bruno's Best LED* | User P/N: | 123.456-78 |
| Supplier manufacturing site: | *Munich, Germany* | User specification #: | EVE-LED-123 |
| Supplier generic P/N: | *EVE-LED* | Required PPAP submission date: | 05.04.2019 |
| Supplier internal P/N: | *EVE20010405* | Robustness level: | 1 |
| Reason for qualification: | Process change #0815 - new epitaxy for EVE-LEDs | Corrosion class: | A |

| Test no. | Test name | Test condition If [mA] | Test condition other | Max. archieved Tj [°] | Max. archieved Ts [°] | Remarks (E.g. test is not applicable; use of generic data) | Est. start | Est. end | # Lots | Samples per lot |
|---|---|---|---|---|---|---|---|---|---|---|
| A1 | PC | | | | | | | | all | all |
| A2a | WHTOL1 | 1000 | 1000h; Ta = 85°; rH=85% | 150 | 125 | | 1. Jan 19 | 1. Mrz 19 | 3 | 26 |
| A2b | WHTOL2 | 10 | 1000h; Ta = 85°; rH=85% | 85 | 85 | | 1. Jan 19 | 1. Mrz 19 | 3 | 26 |
| A2c | $H^3TRB$ | | | | | n.a. because not required for LED | | | - | - |
| A3a | PTC | 800 | 2500cyc; -40°/125°; t on/off 5min; | 150 | 125 | | 1. Nov 18 | 1. Mrz 19 | 3 | 26 |
| A3b | IOL | | | | | n.a. because not required for LED | | | | |
| A4 | TC | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| B1a | HTOL1 | 800 | 4000h; Ta = 115° | 150 | 125 | | 1. Jul 18 | 1. Mrz 19 | 3 | 26 |
| B1b | HTOL2 | | | | | n.a. because no derating | | | | |
| B1c | HTRB | | | | | n.a. because not required for LED | | | | |
| B2 | LTOL | | | | | n.a. because not required for LED | | | | |
| B3 | PLT | 2000 | 1000h; Ta = 55°; tp = 0,01ms; DC = 50% | 135 | 110 | | 1. Jan 19 | 1. Mrz 19 | 3 | 26 |
| C1 | DPA | | | | | for HTOL, WHTOL, PTC | 1. Mrz 19 | 14. Mrz 19 | 1 | 2 each |
| C2 | PD | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C3 | WBP | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C4 | WBS | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C5 | DS | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C6 | TS | | | | | n.a. because SMD | | | | |
| C7 | DEW | | | | | not needed because epoxy casted | | | | |
| C8 | RSH | | | | | n.a. because SMD | | | | |
| C9 | TR | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C10 | SD | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C11 | WG | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C12 | H2S | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C13 | FMG | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| C14 | BF | | | | | n.a. acc. to table 3a Change Guideline | | | | |
| E0 | EV | | | | | | 1. Jun 18 | 14. Jun 18 | 3 | 26 |
| E1 | TEST | | incl. simple functioning/no functioning test at cold and hot temperature acc. 2.3.7. | | | | part of subsequent tests | | | |
| E2 | PV | | | | | | 1. Feb 19 | 14. Feb 19 | 3 | 26 |
| E3 | HBM | | up to 8kV | | | | 1. Feb 19 | 14. Feb 19 | 3 | 10 |
| E4 | CDM | | up to 1kV | | | | 1. Feb 19 | 14. Feb 19 | 3 | 10 |
| G1 | CA | | | | | n.a. because not uncasted | | | | |
| G2 | VVF | | | | | n.a. because not uncasted | | | | |
| G3 | MS | | | | | n.a. because not uncasted | | | | |
| G4 | HER | | | | | n.a. because not uncasted | | | | |
| Additional tests | | | | | | | | | | |
| 1 | HTOL1 | 1000 | 4000h; Ta = 135° | 175 | 135 | Overstress | 1. Jul 18 | 1. Mrz 19 | | |

Failure criteria
(according to AEC-Q102 Appendix 5 if not specified else)

| Parameter | Acceptance Criteria | Remark |
|---|---|---|
| Flux | +/- 20% | |
| Cx & Cy | +/- 0,005 | |
| Vf | +/- 5% | |
| Vf | light / no light | For PTC: measured at Ta= -40° and Ta=-125° after stress |
| Vf min | +/- 5% | |

Comments (e.g. deviation from AEC-Q102 requirements):

| | | | |
|---|---|---|---|
| Prepared by (supplier) | Jane Doe | Approved by (user) | Sonja Chérie |
| Department / function | Quality | Department / function | Quality |
| Date | 9th April 2019 | Date | 9th April 2019 |
| Signature | | Signature | |

* Note: This plan is only an example and does not represent all the required tests in this document.

**Figure A3.1: Example of AEC-Q102 Qualification Test Plan**

This template is available as a stand-alone document that can be downloaded at http://www.aecouncil.com.

## Appendix 4: Data Presentation Format

The supplier is required to complete and submit an Environmental Test Summary and Parametric Verification Summary with each Optoelectronic Semiconductor PPAP submittal. Figure A4.1 is an example of a completed Environmental Test Summary.

In addition, the supplier has to provide test data for each individual part if requested by the user. The individual test data should be provided in graphic format (individual data points). Other formats may be chosen if agreed mutually by the user and the supplier.

Figure A4.2 is an example of a completed Parametric Verification Summary. The format of both summaries shall be followed.

Soft copies of the formats may be found on the AEC website or is available upon request. Other equivalent formats are acceptable if approved by the user.

# Automotive Electronics Council

**Component Technical Committee**

## Qualification Data acc. to AEC-Q102 for Optoelectronic Semiconductor

| | | | |
|---|---|---|---|
| Supplier: | *Bruno's Best LED* | AEC-Q102 revision: | Rev. A |
| Supplier manufacturing site: | *Munich, Germany* | Report number: | BB_20190409 rev.1 |
| Supplier generic P/N: | *EVE-LED* | Lots (number & type): | 1) AC2019001 |
| Supplier internal P/N: | *EVE20010405* | | 2) AC2019002 |
| Reason for qualification: | *Process change #0815 - new epitaxy for EVE-LEDs* | | 3) AC2019003 |

| Test no. | Test name | Test condition: If [mA] | Test condition: other | Max. archieved: Tj [°] | Max. archieved: Ts [°] | Remarks (E.g. test is not applicable; use of generic data) | # Lots | Samples per lot | # failures: elec. | # failures: opt. | # failures: vis. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | PC | | | | | | all | all | 0 | 0 | 0 |
| A2a | WHTOL1 | 1000 | 1000h; Ta = 85°; rH=85% | 150 | 125 | | 3 | 26 | 0 | 0 | 0 |
| A2b | WHTOL2 | 10 | 1000h; Ta = 85°; rH=85% | 85 | 85 | | 3 | 26 | 0 | 0 | 0 |
| A2c | $H^3TRB$ | | | | | n.a. because not required for LED | - | - | - | - | - |
| A3a | PTC | 800 | 2500cyc; -40°/125°; t on/off 5min; | 150 | 125 | | 3 | 26 | 0 | 0 | 0 |
| A3b | IOL | | | | | n.a. because not required for LED | | | | | |
| A4 | TC | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| B1a | HTOL1 | 800 | 4000h; Ta = 115° | 150 | 125 | | 3 | 26 | 0 | 0 | 0 |
| B1b | HTOL2 | | | | | n.a. because no derating | | | | | |
| B1c | HTRB | | | | | n.a. because not required for LED | | | | | |
| B2 | LTOL | | | | | n.a. because not required for LED | | | | | |
| B3 | PLT | 2000 | 1000h; Ta = 55°; tp = 0,01ms; DC = 50% | 135 | 110 | | 3 | 26 | 0 | 0 | 0 |
| C1 | DPA | | | | | for HTOL, WHTOL, PTC | 1 | 2 each | 0 | 0 | 0 |
| C2 | PD | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C3 | WBP | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C4 | WBS | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C5 | DS | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C6 | TS | | | | | n.a. because SMD | | | | | |
| C7 | DEW | | | | | not needed because epoxy casted | | | | | |
| C8 | RSH | | | | | n.a. because SMD | | | | | |
| C9 | TR | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C10 | SD | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C11 | WG | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C12 | H2S | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C13 | FMG | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| C14 | BF | | | | | n.a. acc. to table 3a Change Guideline | | | | | |
| E0 | EV | | | | | | 3 | 26 | 0 | 0 | 0 |
| E1 | TEST | | incl. simple functioning/no functioning test at cold and hot temperature acc. 2.3.7. | | | | part of subsequent tests | | | | |
| E2 | PV | | | | | | 3 | 26 | 0 | 0 | 0 |
| E3 | HBM | | up to 8kV | | | | 3 | 10 | 0 | 0 | 0 |
| E4 | CDM | | up to 1kV | | | | 3 | 10 | 0 | 0 | 0 |
| G1 | CA | | | | | n.a. because not uncasted | | | | | |
| G2 | VVF | | | | | n.a. because not uncasted | | | | | |
| G3 | MS | | | | | n.a. because not uncasted | | | | | |
| G4 | HER | | | | | n.a. because not uncasted | | | | | |
| Additional tests | | | | | | | | | | | |
| 1 | HTOL1 | 1000 | 4000h; Ta = 135° | 175 | 135 | Overstress | 3 | 26 | 4 | 2 | 0 |

Failure criteria
(according to AEC-Q102 Appendix 5 if not specified else)

| Parameter | Acceptance Criteria | Remark |
|---|---|---|
| Flux | +/- 20% | |
| Cx & Cy | +/- 0,005 | |
| Vf | +/- 5% | |
| Vf | light / no light | For PTC: measured at Ta= -40° and Ta=-125° after stress |
| Vf min | +/- 5% | |

| | |
|---|---|
| **AEC-Q102 passed: [yes - no - with restriction]** | **YES** |
| **Robustness level (acc AEC-Q102 appendix 7a) :** | **1** |
| **Corrosion class (acc AEC-Q102 test C12 - H2S) :** | **A** |

Comments (e.g. deviation from AEC-Q102 requirements; use of generic data):

Failures at add. test 1 are caused by thermal overstress after 3000h.

| | | | |
|---|---|---|---|
| Prepared by (supplier) | John Doe | Approved by (supplier) | Jane Doe |
| Department / function | Quality | Department / function | Quality |
| Date | 9th April 2019 | Date | 9th April 2019 |
| Signature | | Signature | |

* Note: This listing of test results is only an example and does not represent all the tests in this document.

**Figure A4.1: Environmental Test Summary Example**

This template is available as a stand-alone document that can be downloaded at http://www.aecouncil.com.

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| **Supplier** | | | | **User Part Number** | | | | |
|---|---|---|---|---|---|---|---|---|
| *Bruno's Best LED* | | | | *5317704* | | | | |
| **Lot Number** | | | | **Temperature** | | | | |
| *BBL160001 (Test lot #1)* | | | | *25°C* | | | | |
| Test Name | Unit | Spec LSL | Spec USL | Min | MAX | MEAN | STD DEV | Cpk |
| Iv | mcd | 1440 | 4000 | 2264 | 2486 | 2522 | 50,4 | 6,51 |
| Vf | V | | 3,8 | 3,3 | 3,3 | 3,3 | 0,02 | 15,2 |
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**Figure A4.2: Parametric Verification Summary Example**

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## Appendix 5: Minimum Parametric Test Requirements and Failure Criteria

For Table 2 Test #E1 (Pre- & Post-Stress Electrical Test), the following electrical and optical parameters shall be used (as a minimum). For LEDs with multiple individually addressable chips (e.g., RGB-LEDs but also multichip LEDs with chips of same color), all chips must be tested individually. For LEDs with a high amount of individually addressable dies (e.g., LEDs for high resolution headlamp matrix function), the electrical testing and the failure criteria may be negotiated between the supplier and the user mutually.

**LEDs:**

<table>
<tr><th>Parameter</th><th>Acceptance criteria</th><th>Remark</th></tr>
<tr><td colspan="3">Parameter to measure at room temperature</td></tr>
<tr><td>Luminous flux or Intensity or Luminance or Radiant power<br><br>(whatever is appropriate)</td><td>+/- 20%<br><br>Note: +/- 30% or +/- 50% may be acceptable for some application (e.g., interior).<br><br>Choice of range to be noticed in the test report.</td><td rowspan="3">To measure at nominal rated current.</td></tr>
<tr><td>Color coordinates Cx & Cy<br>or<br>Dominant wavelength<br>(for direct colors)</td><td>+/- 0.01 according to initial value.<br><br>Note: +/- 0.02 may be acceptable for some application (e.g., interior). Other criteria must be negotiated between the supplier and the user mutually.<br><br>Choice of range to be noticed in the test report.<br><br>or<br><br>+/- 2 nm according to initial value (for dominant wavelength)</td></tr>
<tr><td>Forward voltage Vf</td><td>+/- 10%</td></tr>
<tr><td>Forward voltage Vf</td><td>+/- 10%</td><td>To measure at minimum and maximum rated current.<br>If no minimum drive current is specified, 10% of the nominal current or ≤1mA should be chosen.</td></tr>
<tr><td colspan="3">Parameter to measure at minimum & maximum temperature</td></tr>
<tr><td>Forward voltage Vf</td><td>light / no light</td><td>Applies only to: WHTOL, TC, PTC, VVF, MS, H2S and FMG.<br>To measure at nominal rated current. Consider derating.</td></tr>
</table>

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**Laser Components:**

| Parameter | Acceptance criteria | Remark |
|---|---|---|
| Parameter to measure at room temperature | | |
| Luminous flux or Intensity or radiant power<br><br>For APC laser components: $I_{operating}$<br><br>For pulsed operated laser components: pulse peak power and/or average power<br><br>(whatever is appropriate) | +/- 20%<br>Note: +/- 30% or +/- 50% may be acceptable for some applications. Choice of range to be noticed in the test report.<br><br>Additionally, for APC laser components: not to exceed maximum specified $I_{operating}$ | To measure at nominal rated current.<br><br>For APC laser components: at nominal power. |
| Color coordinates Cx & Cy<br>or<br>Dominant wavelength<br>(for direct colors) | +/- 0.02 according to initial value<br>or<br>+/- 2 nm according to initial value | |
| Forward voltage Vf | +/- 10% | |
| Forward voltage Vf | +/- 10% | To measure at minimum and maximum rated current.<br>If no minimum drive current is specified, 10% of the nominal current should be chosen. |
| Peak luminance<br>(max. luminance over whole light emitting area)<br><br>or<br><br>Average luminance | Same variation as chosen for luminous flux (intensity, radiant power respectively). | **For laser components with remote color conversion only.**<br>**Applies only to HTOL, TC, PTC, VVF, MS, H2S, FMG.**<br>Parameter to be measured at nominal rated current on 3 samples before/after. Choice of measuring area (size and position) to be noticed in the test report. |
| Radiation characteristic<br>(intensity over angle) | n.a. | **For direct color laser components only.**<br>**Applies only to HTOL, TC, PTC, WHTOL.**<br>The radiation characteristic has to be measured before and after the stress test. Exemplary data must be provided if requested by the user. |
| Degree of polarization | n.a. | **For direct color laser components only.**<br>**Applies only to HTOL, TC, PTC, WHTOL.**<br>If specified in datasheet, the degree of polarization has to be measured before and after the stress test. Data must be provided if requested by the user. |
| Parameter to measure at minimum & maximum temperature | | |
| Forward voltage Vf | Vf-check for “open”<br>(“light on/off test”) | Applies only to: WHTOL, TC, PTC, VVF, MS, H2S and FMG<br>To measure below threshold current. |
| Laser safety has to be maintained before and after test. | | |

**Photodiodes:**

| Parameter | Acceptance criteria | Remark |
|---|---|---|
| Parameter to measure at room temperature | | |
| Photo current | +/- 25% | |
| Dark current | maximum acc. to data sheet | No light exposure. |
| Forward voltage | +/- 10% | No light exposure. |
| Parameter to measure at minimum & maximum temperature | | |
| Forward voltage | open / short | |

**Phototransistors:**

| Parameter | Acceptance criteria | Remark |
|---|---|---|
| Parameter to measure at room temperature | | |
| Collector Light Current | +/- 25% | With light exposure. |
| Dark current | maximum acc. to data sheet | No light exposure. |
| Parameter to measure at minimum & maximum temperature | | |
| $V_{CE}$ & $V_{BE}$<br><br>(if applicable and defined in part specification) | open / short | Applies only to: H³RTB, TC, IOL, VVF, MS, H2S and FMG |

# Appendix 6: Destructive Physical Analysis (DPA)

## A6.1 Description

The purpose of this examination is to determine the capability of a device's internal materials, design, and workmanship to withstand forces induced by various stresses induced during environmental testing.

## A6.2 Equipment:

a. Optical microscope having magnification capability of up to 50X
b. De-capsulation equipment
c. Cross section equipment

## A6.3 Procedure:

a. Parts selected for this test must have successfully completed environmental testing as defined in Table 2, respectively Table 3a-c (Process Change Guidelines for the Selection of Tests) of AEC-Q102.
b. The parts shall be opened or de-capsulated in order to expose the internal die/substrate and determine the extent of any mechanical or chemical damage. The process used to de-capsulate the device must insure that it does not cause degradation affecting the issue under investigation. The internal die or substrate must be completely exposed and free of packaging material.
c. The parts shall be examined under a magnification of up to 50X to the criteria listed in Section A6.4, herein.
d. A cross section shall be done to analyze critical die structures (e.g., metallization layers, die attach, etc.), wire bonding connection and further critical internal component structures. For hermetic packages this implies the connection stem-cap, stem-leads and cap-window.
e. All parts, failing any qualification test, shall be analyzed to determine the cause of the failure. A Failure Analysis Report documenting this analysis shall be prepared on all failures. If the analysis shows that the failure was caused by the package opening process, the test shall be repeated on a second group of parts.
f. Risk evaluation shall be done for failed parts and reported to the user. Generic data, additional reliability tests and/or common literature may be used.

## A6.4 Failure Criteria:

Parts shall be considered failed if they exhibit any of the following:

a. Visible evidence of non-conforming to the devices' Certificate of Design, Construction and Qualification.
b. Visible evidence of corrosion, contamination, delamination or metallization voids. If the supplier can show by means of additional testing or analysis that these abnormalities have no impact on product reliability and lifetime, the part may be considered as passed. Nevertheless, the abnormality has to be mentioned within the test report. Details of additional testing or analysis has to be provided to the user if requested.
c. Visible evidence of die/substrate cracks or defects (e.g., scratches, glassivation, etc.).
d. Visible evidence of wire, die, or termination bond defects.
e. Visible evidence of dendrite growth or electromigration.

# Appendix 7: AEC-Q102 and the Use of Mission Profiles

## A7.1 SCOPE

Successful completion of the test requirements in Table 2 allows the claim to be made that the part is AEC Q102 qualified. Additional testing may be agreed between Component Manufactures and Tier 1 Component Users depending on more demanding application environments. To address these more stringent conditions, application based Mission Profiles may be used for a reliability capability assessment.

A mission profile is the collection of relevant environmental and functional loads that a component will be exposed to during its use lifetime.

### A7.1.1 Purpose

This appendix provides information on an approach that can be used to assess the suitability of a component for a given application and its mission profile for unique requirements. The benefit of applying this approach is that, in the end, the reliability margin between the component (specification) space and the application (condition) space may be shown.

- Section A7.2 demonstrates the relation between AEC-Q102 stress conditions / durations and a typical example of a set of use life time and loading conditions.
- Section A7.3 describes the approach, supported by flow charts, which can be used for a reliability capability assessment starting from a mission profile description.

### A7.1.2 References

- **SAE J1879/J1211/ZVEI** Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications
- **JEDEC JEP122** Failure Mechanisms and Models for Semiconductor Devices

## A7.2 BASE CONSIDERATIONS

### A7.2.1 Use Lifetime and Mission Profile

The use lifetime assumptions drawn here are an example used for demonstration purpose only. Many typical mission profiles will differ in one or more characteristics from what is shown below.

- service lifetime in years
- engine on-time in hours
- engine off time {idle} in hours
- non-operating time in hours
- number of engine on-off cycles
- service mileage

The mission profile itself is generated by adding information on thermal, electrical, mechanical and any other forms of loading under use conditions to the above lifetime characteristics. Examples of these and how they relate to the test conditions in Table 2 are shown in Table A7.1.

### A7.2.2 Relation to AEC-Q102 Stress Test Conditions and Durations

The basic calculations in Table A7.1 for each of the major stress tests demonstrate how one can derive suitable test conditions for lifetime characteristics based on reasonable assumptions for the loading. Caution should always be taken on use of excessive test conditions beyond those in Table 2, because they may induce unrealistic fail mechanisms and/ or acceleration.

### A7.3 METHOD TO ASSESS A MISSION PROFILE

This section demonstrates how to perform a more detailed reliability capability assessment in cases where the application differs significantly from existing and proven situations:

- Application has a demanding loading profile
- Application has an extended service lifetime requirement
- Application has a more stringent failure rate target over lifetime

These considerations may result in extended test durations. In addition, there may be components manufactured in new technologies and/or containing new materials that are not yet qualified. In such cases, unknown failure mechanisms may occur with different times-to-failure which may require different test methods and/or conditions and/or durations.

For these cases, two flow charts are available to facilitate both Tier 1 and Component Manufacturing in a reliability capability assessment:

- Flow Chart 1 in Figure A7.1, describes the process at Component Manufacturer to assess whether a new component can be qualified by AEC-Q102.
- Flow Chart 2 in Figure A7.2, describes (1) the process at Tier 1 to assess whether a certain electronic component fulfills the requirements of the mission profile of a new Electronic Control Unit (ECU); and (2) the process at Component Manufacturer to assess whether an existing component qualified according to AEC-Q102 can be used in a new application.

For details on how to apply this method, please refer to SAE J1879, SAE J1211 and/or ZVEI Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications.

In summary, the flow charts result in the following three clear possible conclusions:

[A] AEC-Q102 test conditions do apply.
[B] Mission Profile specific test conditions may apply.
[C] Robustness Validation may be applied with detailed alignment between Tier1 and Component Manufacturer.

In addition, not shown in the flow charts, the expected end of life failure rate may be an important criterion. Regarding failure rates, the following points should be considered:

- No fails in 78 devices (26 devices from 3 lots) are applied as pass criteria for the major environmental stress tests. This represents an LTPD (Lot Tolerance Percent Defective) = 3, meaning a maximum of 3% failures at 90% confidence level.
- This sample size is sufficient to identify intrinsic design, construction and/or material issues affecting performance.
- This sample size is NOT sufficient or intended for process control or PPM evaluation. Manufacturing variation failures (low ppm issues) are achieved through proper process controls and/or screens such as described in AEC-Q001 and -Q002.
- Three lots are used as a minimal assurance of some process variation between lots. A monitoring process has to be installed to keep process variations under control.
- Sample sizes are limited by part and test facility costs, qualification test duration and limitations in batch size per test.

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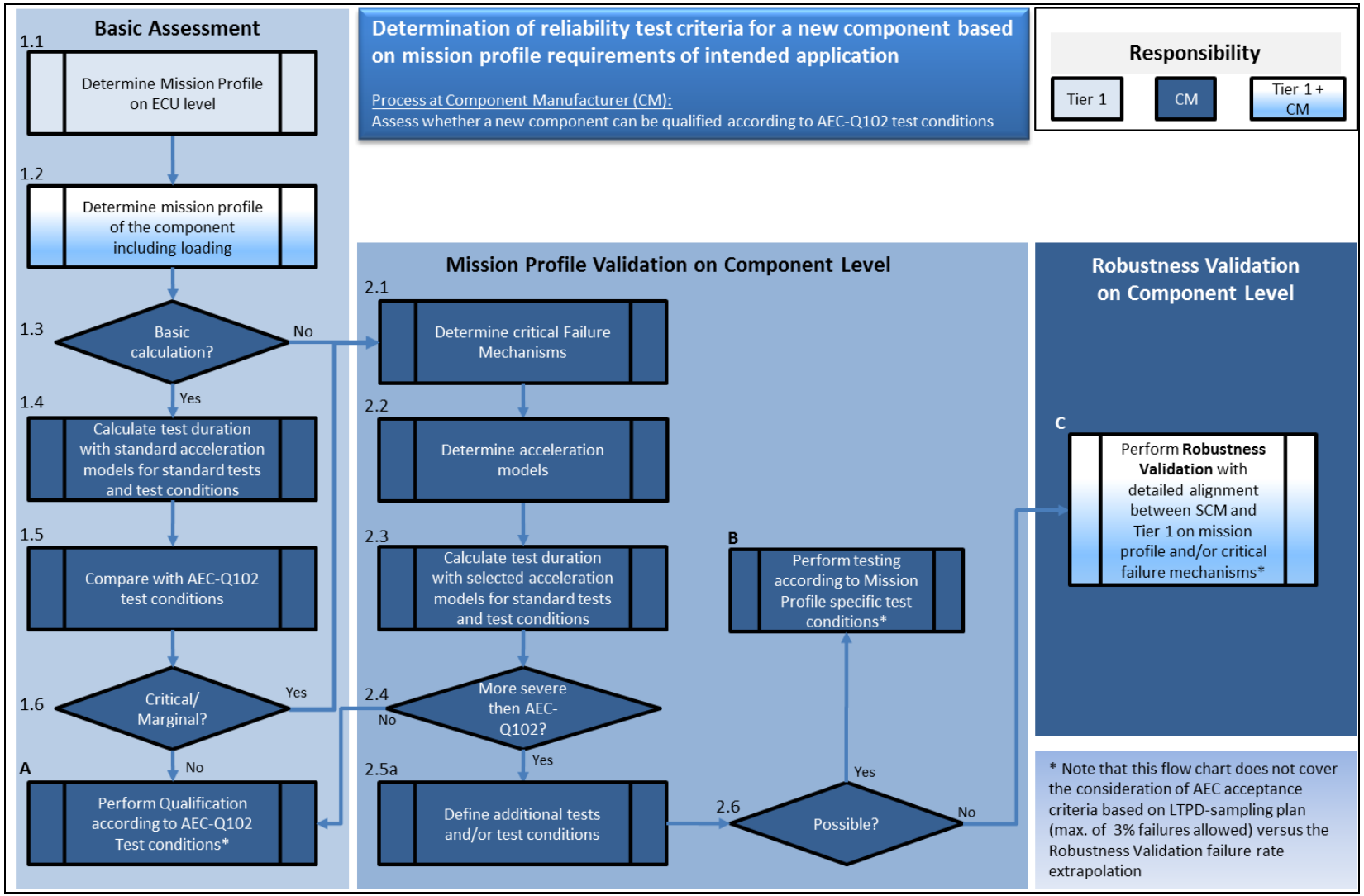


**Figure A7.1: Flow Chart 1 – Reliability Test Criteria for New Component**

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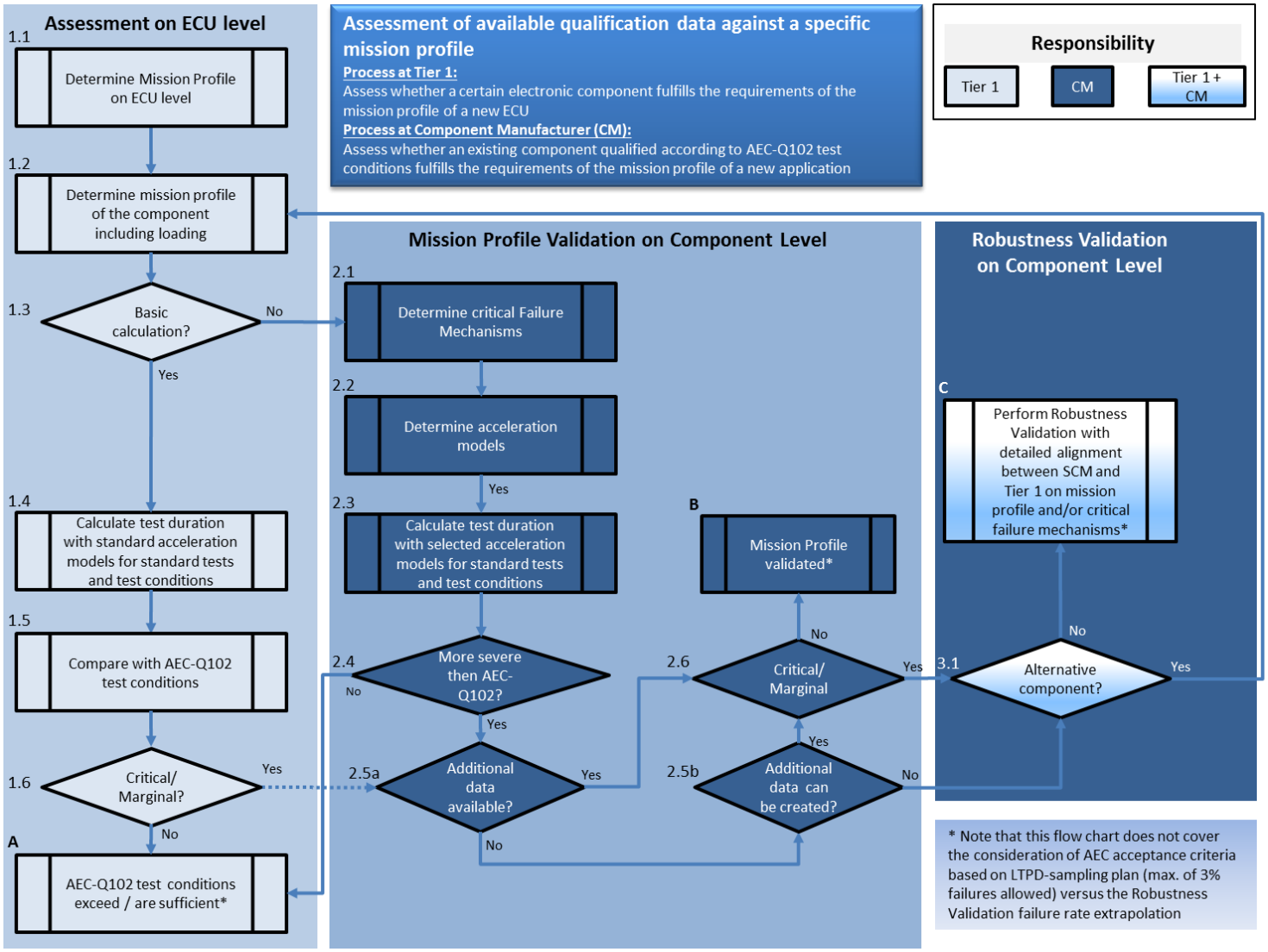


**Figure A7.2: Flow Chart 2 – Assessment of Existing, Qualified Component**

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## Table A7.1: Example Calculations for AEC-Q102 Tests for Optoelectronic Semiconductors

| Loading | Mission Profile Input | Stress Test | Stress Conditions | Acceleration Model (all temperatures in K, not in °C) | Model Parameters | Calculated Test Duration | Q102 Test Duration |
|---|---|---|---|---|---|---|---|
| **Operation** | $t_u$ = 12,000 h (average operating use time over 15 years)<br><br>$T_u$ = 100 °C (average junction temperature in use environment) | High Temperature Operating Life (HTOL)<br><br>or<br><br>High Temperature Reverse Bias (HTRB) | $T_t$ = 150 °C (junction temperature in test environment) | Arrhenius<br>$A_f = \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$<br><br>Also applicable for High Temperature Storage Life (HTSL) | $E_a$ = 0.7 eV (activation energy; 0.7 eV is a typical value, actual values depend on failure mechanism and range from -0.2 to 1.4 eV)<br><br>$k_B$ = 8.61733 x $10^{-5}$ eV/K (Boltzmann's Constant) | $t_t$ = 916 h (test time)<br>$t_t = \frac{t_u}{A_f}$ | 1000 h |
| **Thermo-mechanical** | $n_u$ = 54,750 cycles (number of engine on/off cycles over 15 years of use)<br><br>$\Delta T_u$ =70 K (average thermal cycle temperature change in use environment) | Temperature Cycling (TC) | $\Delta T_t$ =205 K (thermal cycle temperature change in test environment: -55 °C to 150 °C) | Coffin Manson<br>$A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$ | m = 4 (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials) | $n_t$ =744 cycles (number of cycles in test)<br>$n_t = \frac{n_u}{A_f}$ | 1000 cycles |
| | $n_u$ = 54,750 cycles (number of engine on/off cycles over 15 years of use)<br><br>$\Delta T_u$ =55 K for solder die attach (average thermal cycle temperature change in use environment) | Intermittent Operational Life (IOL) | $\Delta T_t$ =100°C (thermal cycle temperature change in test environment: 25 °C to 125 °C) | Coffin Manson<br>$A_f = \left(\frac{\Delta T_t}{\Delta T_u}\right)^m$<br><br>Also applicable for Power Temperature Cycle (PTC)<br><br>Remark: The use of a Coffin-Manson model may not be appropriate to reflect time dependence of material behavior. | m = 2.5 (Coffin Manson exponent; 4 is to be used for cracks in hard metal alloys, actual values depend on failure mechanisms and range from 1 for ductile to 9 for brittle materials) | $n_t$ =12,283 cycles (number of cycles in test)<br>$n_t = \frac{n_u}{A_f}$ | 1000 cycles |

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## Table A7.1: Example Calculations for AEC-Q102 Tests for Optoelectronic Semiconductors (continued)

| Loading | Mission Profile Input | Stress Test | Stress Conditions | Acceleration Model (all temperatures in K, not in °C) | Model Parameters | Calculated Test Duration | Q102 Test Duration |
|---|---|---|---|---|---|---|---|
| **Humidity** | Engine Non-operating:<br><br>$t_u$ = 119,400 hours (average engine off time over 15 years)<br><br>$RH_u$ = 75 % (average relative humidity in off mode)<br><br>$T_u$ = 30 °C (average junction temperature in engine off mode) | Wet High Temperature Operating Life (WHTOL)<br><br>or<br><br>High Humidity High Temperature Reverse Bias ($H^3TRB$) | $RH_t$ = 85% (relative humidity in test environment)<br><br>$T_t$ = 85°C (ambient temperature in test environment) | Hallberg-Peck<br>$A_f = \left(\frac{RH_t}{RH_u}\right)^p \bullet \exp\left[\frac{E_a}{k_B} \bullet \left(\frac{1}{T_u} - \frac{1}{T_t}\right)\right]$ | p = 3<br>Reference Hallberg-Peck (1991)<br><br>$E_a$ = 0.9 eV<br>Reference Hallberg-Peck (1991)<br><br>$k_B$ = 8.61733 x $10^{-5}$ eV/K (Boltzmann's Constant) | $T_t$ = 413 h<br>$t_t = \frac{t_u}{A_f}$ | 1000 h |

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## Appendix 7a: Reliability Validation for Optoelectronic Semiconductors

The progress in lighting technology is rapid. It is getting more and more common that new kind of optoelectronic semiconductors and technologies are developed in parallel with lighting application. This makes it sometimes difficult to follow the Robustness Validation approach, described in Appendix 7.

For optoelectronic semiconductors, the use lifetime strongly depends on the kind of application. So interior lighting mostly has different requirements compared to exterior rear and exterior front lighting application. In addition, application for trucks may have different requirements compared to the majority of personal cars. The matrix here is seen to be a typical set of longtime reliability tests safeguarding the various lifetime reliability requirements. If reliability cannot be proven by the classical Robustness Validation approach, this set of tests can be chosen alternatively.

| **LED & Laser Component** | | | | |
|---|---|---|---|---|
| **Test** | **Condition** | **RV-level 2** | **RV-level 1** | **RV-level 0** |
| | Per AEC-Q102 | Extreme long life exterior | Long life exterior | Interior and normal life exterior |
| HTOL 1 | See test B1a | 10000 hours | 4000 hours | 1000 hours |
| HTOL 2 | See test B1b | 10000 hours | 4000 hours | 1000 hours |
| PTC | See test A3a | 2500 cycles | 2500 cycles | 1000 cycles |

| **Photodiode and Phototransistor** | | | | |
|---|---|---|---|---|
| **Test** | **Condition** | **RV-level 2** | **RV-level 1** | **RV-level 0** |
| | Per AEC-Q102 | Extreme long life | Long life | Normal life |
| $H^3TRB$ | See test A2c | Application specific | 2000 hours | 1000 hours |

Note: DPA needed after reaching final RV-level test duration
Sample size: According to table 2. For > 1000h / cycles (RV-level 1 & 2) reduction to 30 parts (3 lots 10 pcs. each) possible
Failure criteria: 0 failures according to AEC-Q102 Appendix 5 allowed

RV level 1 & 2 are additional tests for robustness evaluation only. Passing tests, defined in Table 2 of base document AEC-Q102, (RV-level 0) qualifies the part already to AEC-Q102.

Especially but not limited for RV1 & RV2 it is strongly recommended to determine failure modes and acceleration parameter by the help of overstress tests. The following tests, derived from SAE/USCAR-33, are recommended:

- High Temperature Operating Life
  Tj = max. specified Tj +15 °C (Tj +30 °C for Low and Mid Power LEDs < 1 W)
  $I_F$ = 1.25x max. specified $I_F$ ($I_F$ = 1.5x for Low and Mid Power LEDs < 1 W)

- High Humidity & Temperature Operating Life
  85 °C 85% RH ambient
  $I_F$ = 1.25x max. specified $I_F$ ($I_F$ = 1.5x for Low and Mid Power LEDs < 1 W)

- Power Temperature Cycle
  $T_S$ = -40 °C to 125 °C
  10 minutes dwell, 20 minutes transfer time
  2 minutes power ON / OFF each
  $I_F$ = 1.3x max. specified $I_F$ ($I_F$ = 1.5x for Low and Mid Power LEDs < 1 W)

- Temperature Shock
  -55 °C/150 °C
  15 minutes dwell, <10 second transfer time

  Sample size: 78 parts (3 lots 26 pcs. each)
  Stress duration: 50% of samples size failed, 1500 hours / cycles maximum
  Perform Pre- and Post-Stress Electrical and Photometric Test and Pre-conditioning per AEC-Q102
  For failure criteria, follow AEC-Q102 Appendix 5
  Destructive Physical Analysis (DPA) shall be performed on 2 (failed) parts each test

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# Revision History

| Rev # | Date of change | Brief summary listing affected sections |
|---|---|---|
| - | Mar. 15, 2017 | Initial Release. |
| A | Apr. 6, 2020 | Complete Revision. Revised Sections 1, 1.2.2, 1.2.4, 1.3.3, 2.1, 2.2, 2.3.1, 2.3.7, 2.4, 2.5, 2.7, 3.2.1, 3.2.3, 3.3, 4.2, 4.3, Appendix 1, Appendix 2, Appendix 5, Appendix 6, Appendix 7, Figures A3.1 and A4.1, and Tables 2 and 3a-c. Added Section 4.5, Figures 1a and 4. Deleted Table 2a. |